

0015235 002000
000260 50025160

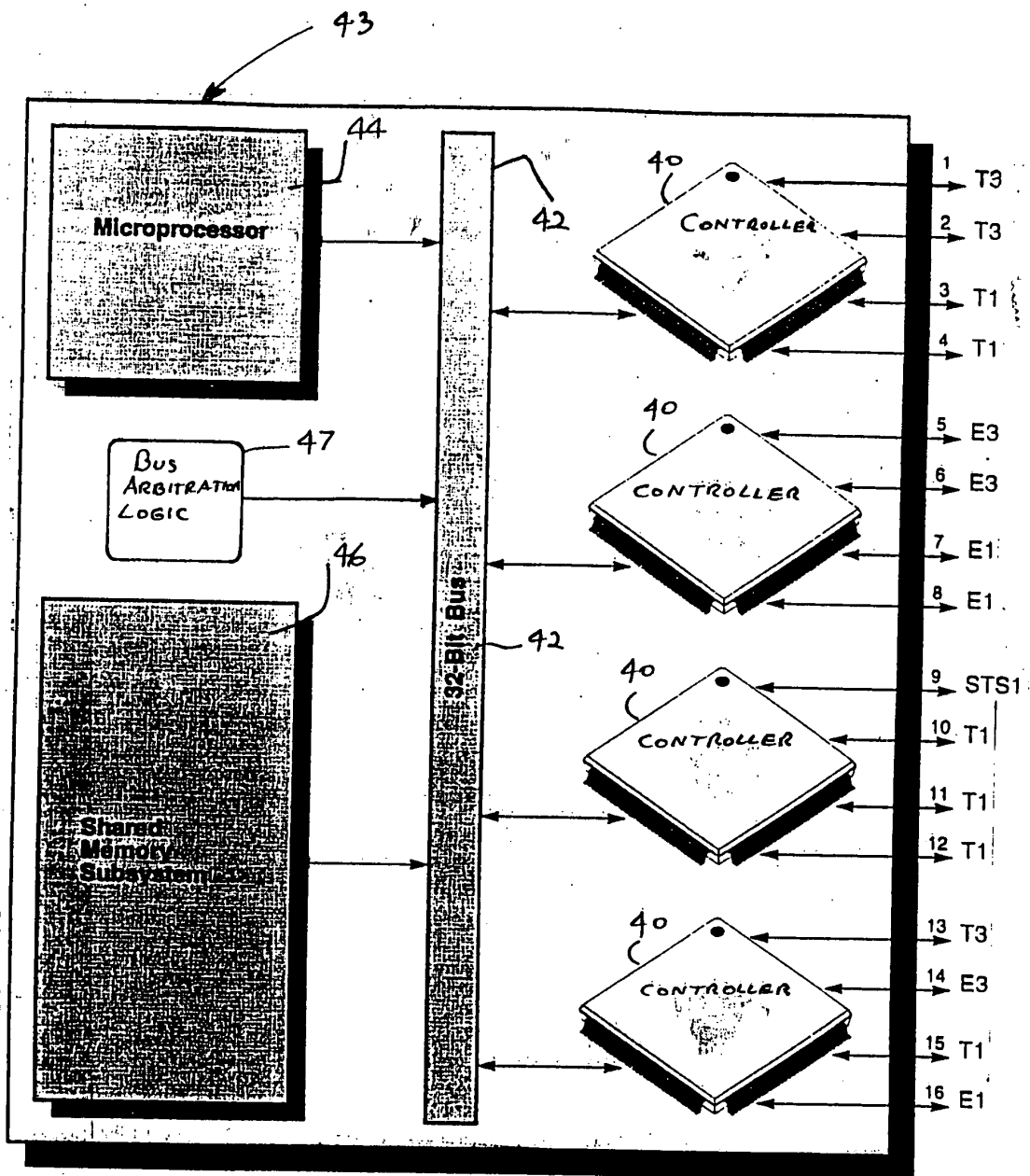


FIG. 1

600200-5265100

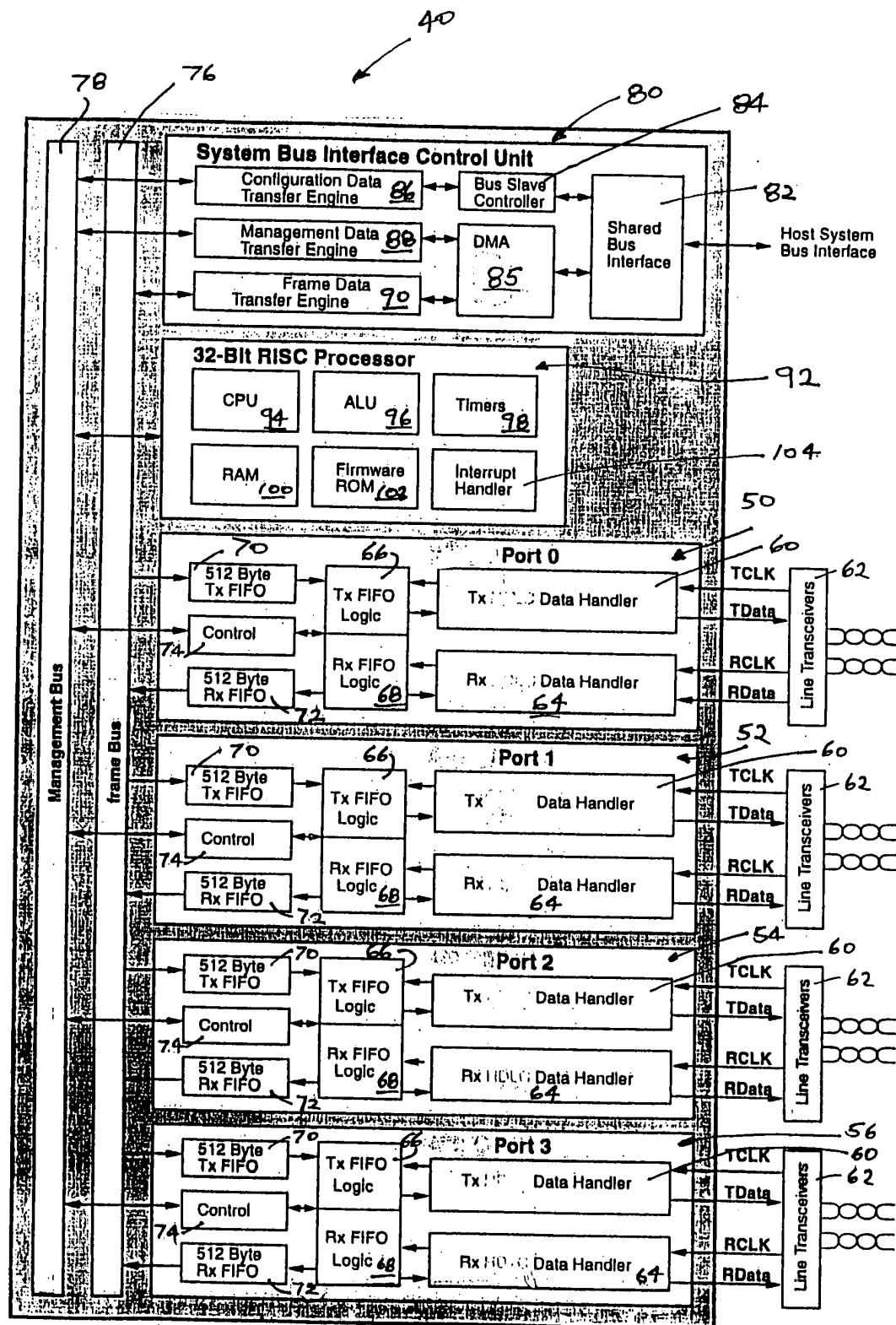
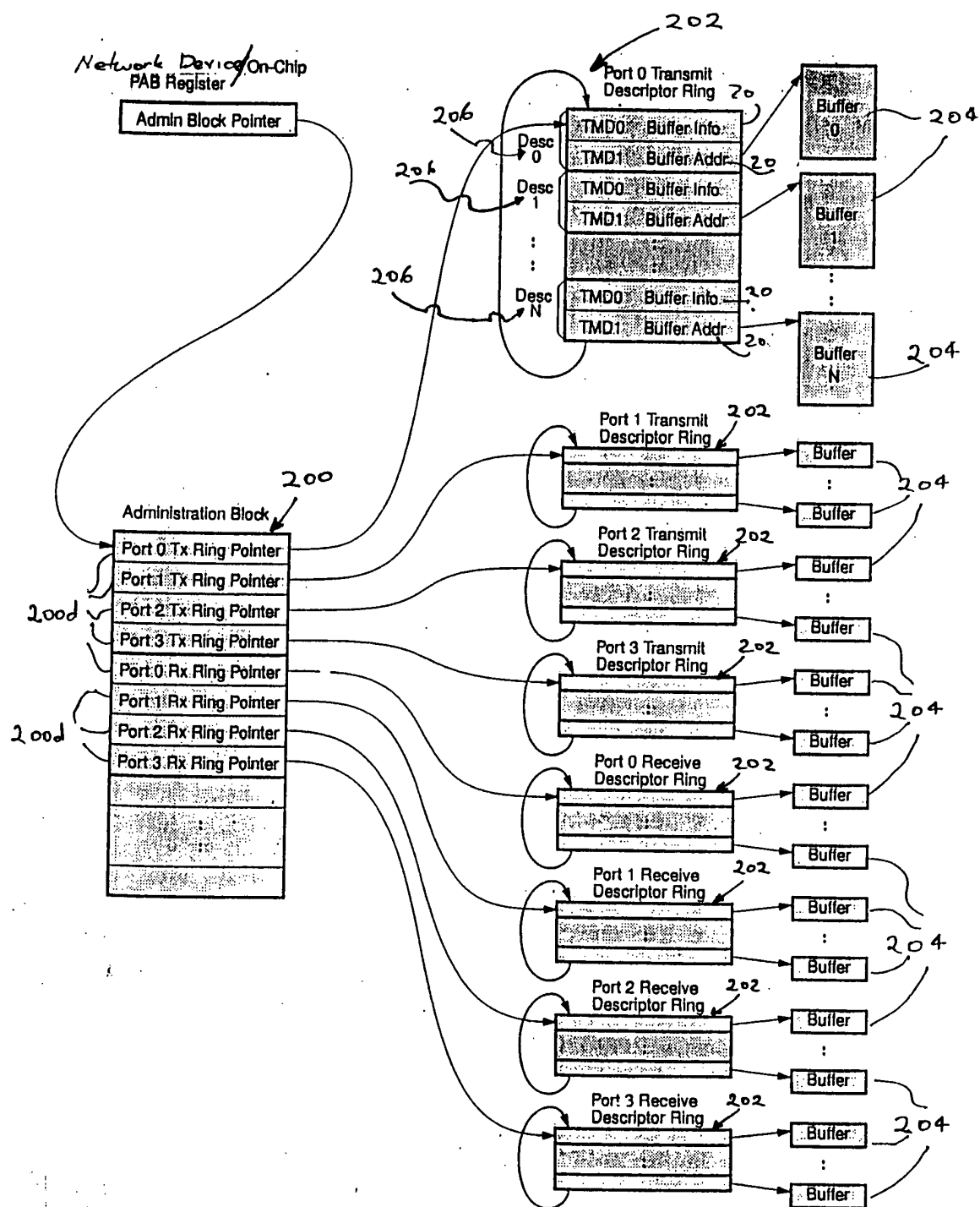


FIG. 2

Network Device On-Chip
PAB Register



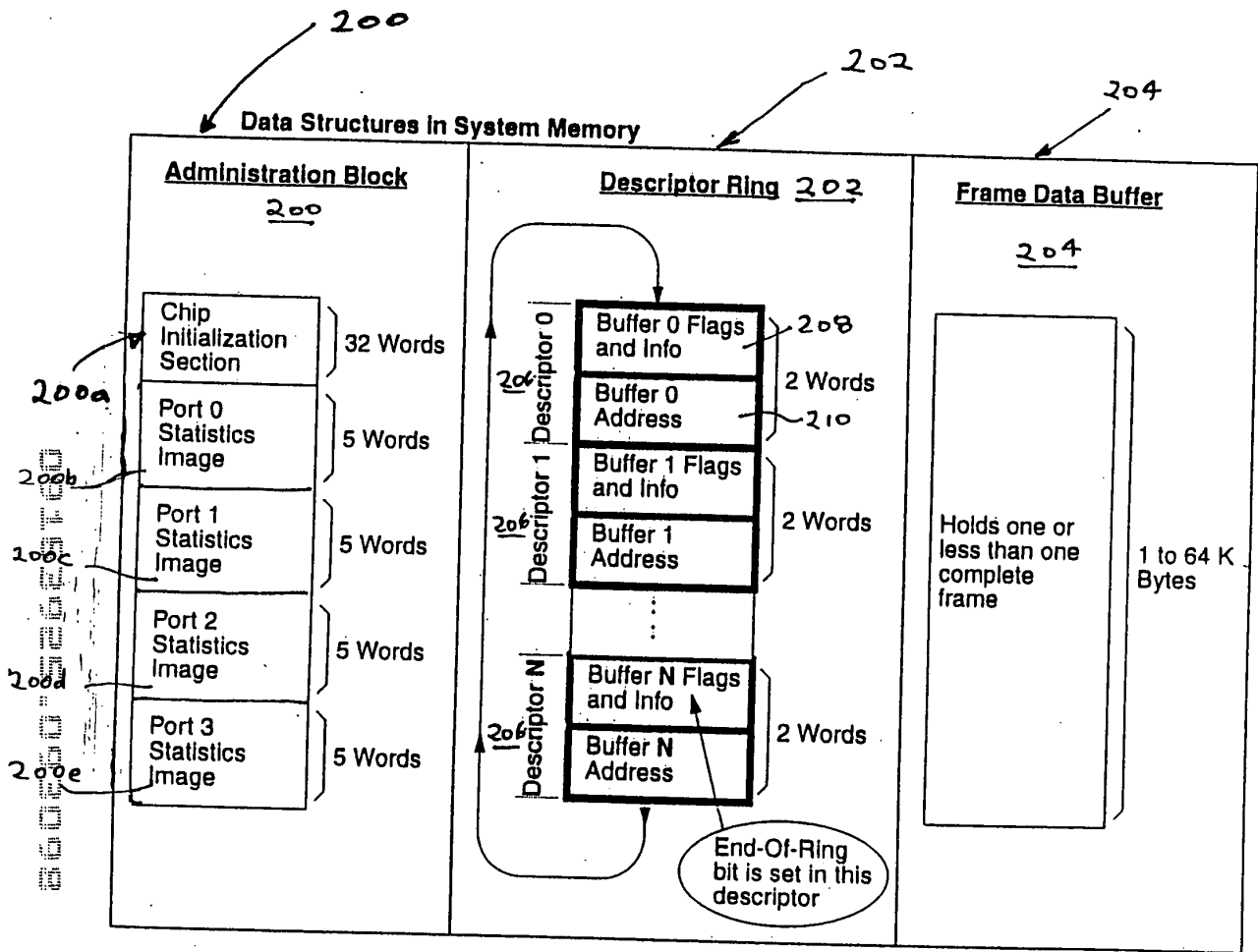


FIG. 4

SECRET

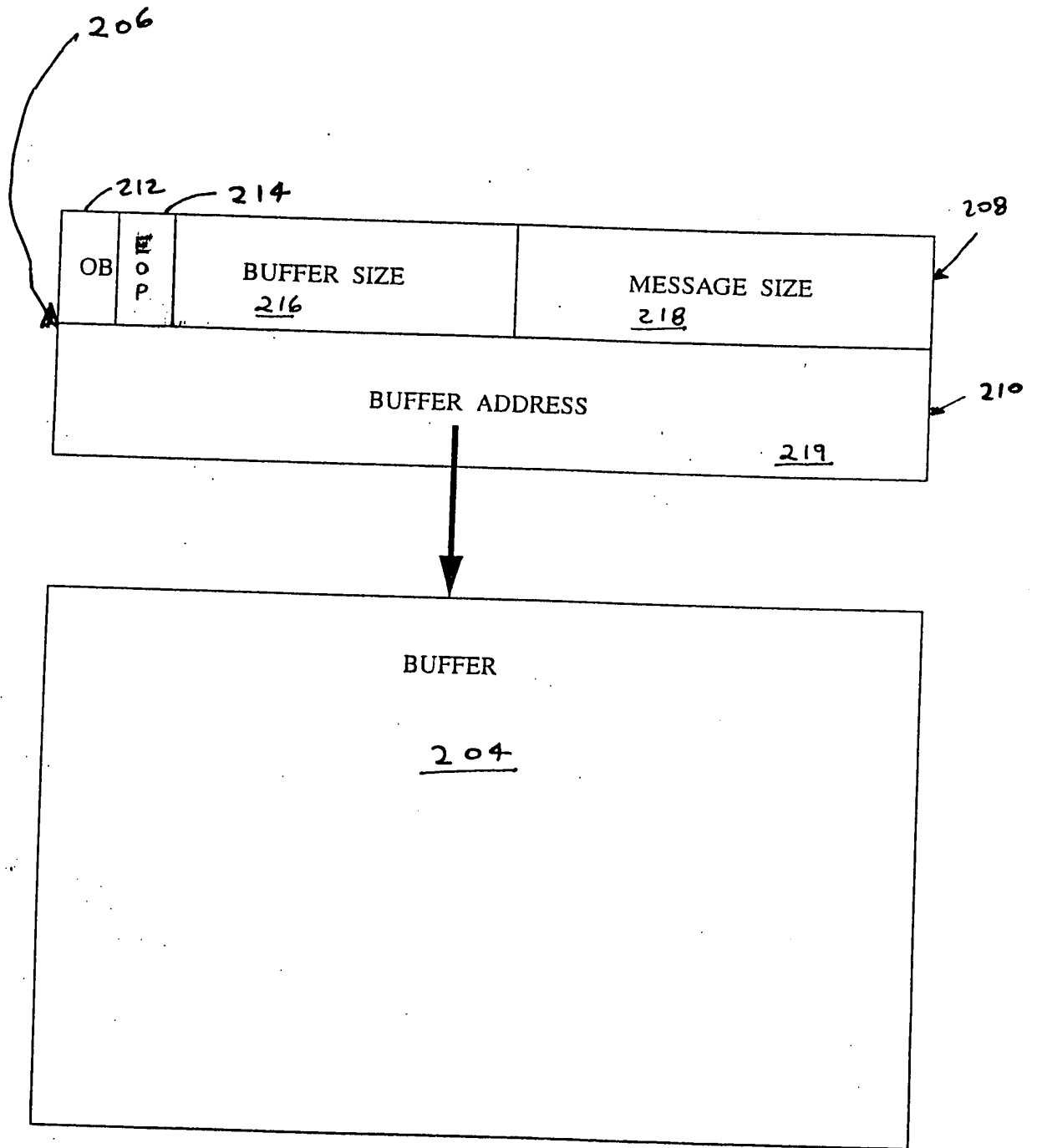


FIG. 5

001498-0000-300000

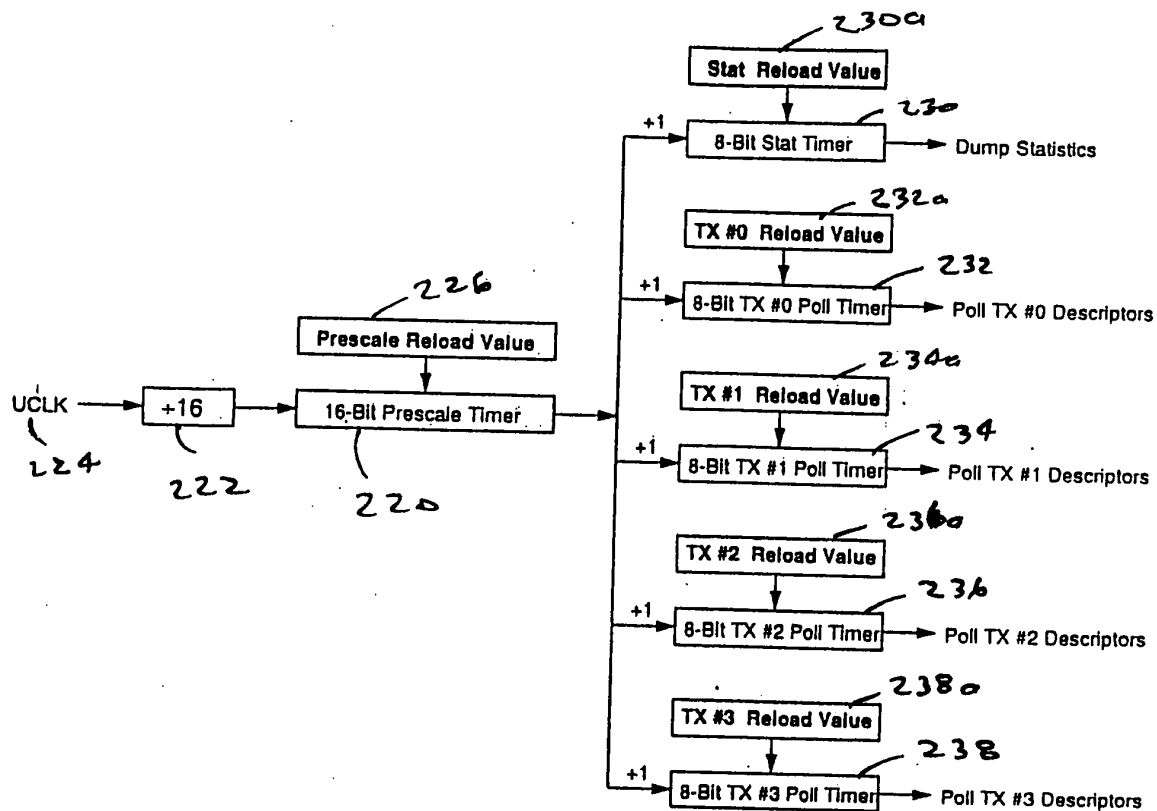


FIG. 6

00163000-000000

200a

200b

200c

200d

200e

200f

200g

200h

200i

Relative Address	Byte 3	Byte 2	Byte 1	Byte 0
PAB + 0	Port 0 Tx Top-Of-Ring Descriptor Pointer			
PAB + 4	Port 1 Tx Top-Of-Ring Descriptor Pointer			
PAB + 8	Port 2 Tx Top-Of-Ring Descriptor Pointer			
PAB + 12	Port 3 Tx Top-Of-Ring Descriptor Pointer			
PAB + 16	Port 0 Rx Top-Of-Ring Descriptor Pointer			
PAB + 20	Port 1 Rx Top-Of-Ring Descriptor Pointer			
PAB + 24	Port 2 Rx Top-Of-Ring Descriptor Pointer			
PAB + 28	Port 3 Rx Top-Of-Ring Descriptor Pointer			
PAB + 32	Prescale Timer Reload Value		Stat Timer Reload Value	Timer Enables
PAB + 36	Port 3 TX Poll Timer Reload Value	Port 2 TX Poll Timer Reload Value	Port 1 TX Poll Timer Reload Value	Port 0 TX Poll Timer Reload Value
PAB + 40	Port 3 TX Burst Size	Port 2 TX Burst Size	Port 1 TX Burst Size	Port 0 TX Burst Size
PAB + 44	Port 3 RX Burst Size	Port 2 RX Burst Size	Port 1 RX Burst Size	Port 0 RX Burst Size
PAB + 48	Reserved	Reserved	UCLK Period (nanoseconds)	Statistics Burst Size
PAB + 52	Port 1 N1		Port 0 N1	
PAB + 56	Port 3 N1		Port 2 N1	
PAB + 60	Port #0 Buffer Size		TX Ring Size	RX Ring Size
PAB + 64	Port #1 Buffer Size		TX Ring Size	RX Ring Size
PAB + 68	Port #2 Buffer Size		TX Ring Size	RX Ring Size
PAB + 72	Port #3 Buffer Size		TX Ring Size	RX Ring Size
PAB + 76	Reserved			
PAB + 80	Reserved			
PAB + 84	Reserved			
PAB + 88	Reserved			
PAB + 92	Reserved			
PAB + 96	Reserved			
PAB + 100	Reserved			
PAB + 104	Reserved			
PAB + 108	Reserved			
PAB + 112	Reserved			
PAB + 116	Reserved			
PAB + 120	Reserved			
PAB + 124	Reserved			

FIG 7

00000000 00000000

Port 0 Relative Address	Byte 3	Byte 2	Byte 1	Byte 0	PORT
PAB + 128	Bad Frames Received				PORT #0
PAB + 132	Aborted Frames				
PAB + 136	Frames Exceeding N1 Received				
PAB + 140	Reserved				
PAB + 144	Reserved				
PAB + 148	Bad Frames Received				PORT #1
PAB + 152	Aborted Frames				
PAB + 156	Frames Exceeding N1 Received				
PAB + 160	Reserved				
PAB + 164	Reserved				
PAB + 168	Bad Frames Received				PORT #2
PAB + 172	Aborted Frames				
PAB + 176	Frames Exceeding N1 Received				
PAB + 180	Reserved				
PAB + 184	Reserved				
PAB + 188	Bad Frames Received				PORT #3
PAB + 192	Aborted Frames				
PAB + 196	Frames Exceeding N1 Received				
PAB + 200	Reserved				
PAB + 204	Reserved				

FIG. 8

[illegible]

Bit #	Field	Name	Description
31	PPA	Provider Primitive Available	(1=available; 0=no primitive) Set by the device when the PCR register is written by the firmware. The setting of this bit will also cause the PINT bit of the MIR to be set automatically. This bit is cleared by the DMA when the host reads this register.
30:24	PPRIM	Provider Primitive Command	(7-bit binary value) This field is an outgoing (Firmware to Host) primitive command. The meaning is strictly determined by the firmware.
23:16	PPARM	Provider Primitive Parameter	(8-bit binary value) This is a firmware defined parameter field corresponding to the provider primitive command.
15	HPA	Host Primitive Available	(1=available; 0=no primitive) Set by the device when the PCR register is written by the host. The setting of this bit can result in a CPC interrupt if enabled. This bit is cleared by the DMA when the firmware reads this register.
14:8	HPRIM	Host Primitive Command	(7-bit binary value) This field is an incoming (Host to Firmware) primitive command. The meaning is strictly determined by the firmware.
7:0	HPARM	Host Primitive Parameter	(8-bit binary value) This is a firmware defined parameter field corresponding to the host primitive command.

FIG. 8A

10x2A1 MIR – Master Interrupt Register

DMA	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	PINT	SPURINT	SDRIFT3	ECN3	FAN3	SHL3	TINT3	RINT3	MERR	PPLOST	SDRIFT2	ECN2	FAN2	SHL2	TINT2	RINT2	SERR	HPLOST	SDRIFT1	ECN1	FAN1	SHL1	TINT1	RINT1	WERR	Spare	SDRIFT0	ECN0	FAN0	SHL0	TINT0	RINT0
Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Host Access	Read-Clear (No Write)																															
CPC Access	Read-Zeros	Read-Zeros / Write-Ones							Read-Zeros	Read-Zeros / Write-Ones							Read-Zeros	Read-Zeros / Write-Ones							Read-Zeros	Read-Zeros / Write-Ones						

Bit #	Field	Name	Description
31	PINT	Primitive Interrupt	(1=event; 0=no event) Set by the device when the firmware writes a new provider primitive into the Primitive Command Register (upper half).
23	MERR	Memory Error	(1=event; 0=no event) Set by the device when an RTIME Ready Timeout has occurred as defined and established in the System Mode Register (SMR).
15	SERR	System Error	(1=event; 0=no event) Set by the device when an STIME System Timeout has occurred as defined and established in the System Mode Register (SMR).
7	WERR	Configuration Write Error	(1=event; 0=no event) Set by the device when the host has attempted to write to a register location which is inaccessible by the host. This bit will never be set when host access is unlocked via the KEY field of the LOCK Register.
30	SPURINT	Spurious CPC Interrupt	(1=event; 0=no event) Set by the CPC firmware indicating the reception of an invalid internal CPC interrupt. This is a device hardware fault and should never occur.
22	PPLOST	Provider Primitive Lost	(1=event; 0=no event) Set by the device when the firmware writes a new provider primitive over one that has not yet been read by the host. This condition is detected by testing the PPA bit of the Primitive Command Register (PCR).
14	HPLOST	Host Primitive Lost	(1=event; 0=no event) Set by the device when the host writes a new host primitive over one that has not yet been read by the firmware. This condition is detected by testing the HPA bit of the Primitive Command Register (PCR).
6	Spare		
29, 21, 13, 5	SDRIFT	Port <i>n</i> Statistic Drift	(1=event; 0=no event) Set by the CPC firmware when conditions in the corresponding port have been reached where statistical information might be lost. This will only happen when receive congestion is occurring such that frames are being lost due to lack of available space in the port's receive FIFO.
28, 20, 12, 4	ECN	Port <i>n</i> Early Congestion Notification	(1=event; 0=no event) Set by the CPC firmware for advanced host notification of congestion in the corresponding port's receiver. Congestion occurs when a unit is forced to drop a received frame due to lack of available space in the Rx FIFO.
27, 19, 11, 3	FAN	Frame Address Notification	(1=event; 0=no event) Set by the device to notify the host that the address fields are present in the frame buffer.
26, 18, 10, 2	SHL	Port <i>n</i> Statistic Half-Life	(1=event; 0=no event) Set by the CPC firmware when one or more of the corresponding port's statistics has passed the half-full mark – defined as the most-significant-bit of a statistic changing polarity (0-to-1 or 1-to-0) due to the last update.
25, 17, 9, 1	TINT	Port <i>n</i> Transmit Interrupt	(1=event; 0=no event) Set by the device whenever the transmission of one or more frames has been completed. For a successfully transmitted frame this interrupt signals that the frame has cleared the chip.
24, 16, 8, 0	RINT	Port <i>n</i> Receive Interrupt	(1=event; 0=no event) Set by the device whenever a receive frame has been completely transferred from the corresponding port to the host system. This means a frame has been transferred to System Memory. If the reception of bad frames (RBUFF=0 in the SMR register) has been disabled then no RINT will be generated in the event of bad frames.

FIG. 8B

802.3 DATALINK LAYER HEADER (18 Bytes)

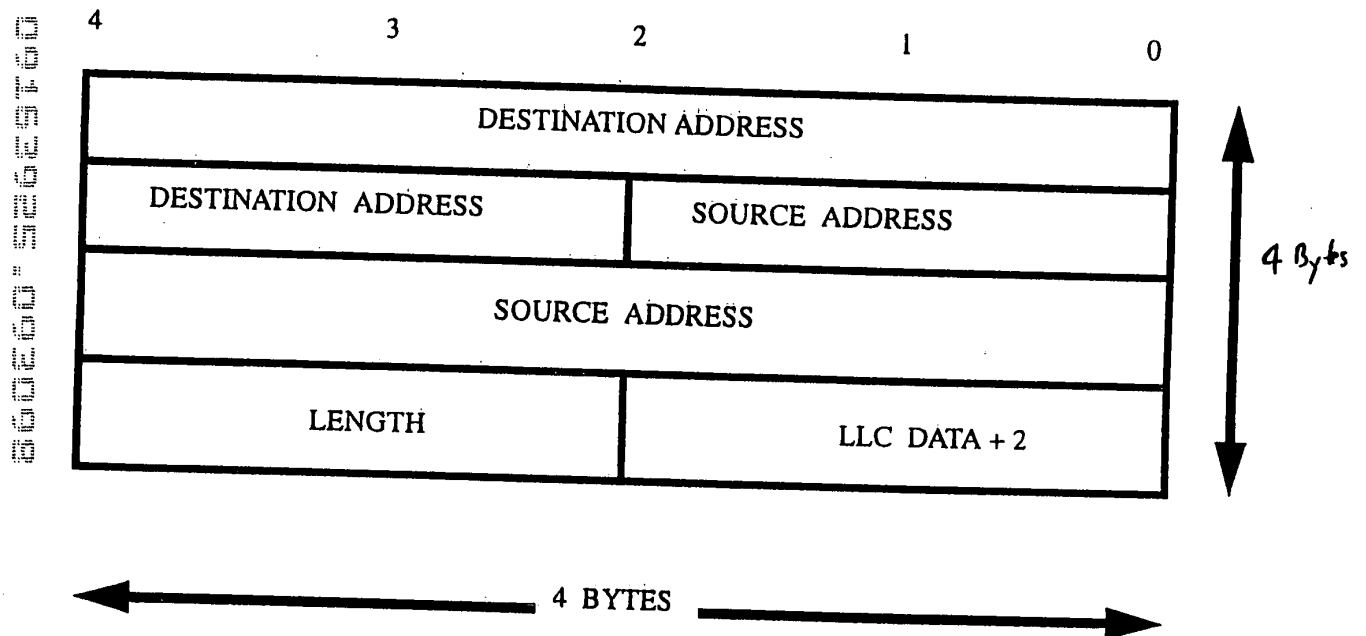


FIG. 10

INTERNET IP HEADER (20 Bytes)

66060 36360

VER/HEADER	TYPE OF SERVICE	16-BIT TOTAL LENGTH (IN BYTES)
16-BIT IDENTIFICATION		3-BIT FLAGS/13-BIT FRAGMENT OFFSET
TTL	8-BIT PROTOCOL	16-BIT HEADER CHECKSUM
32-BIT SOURCE IP ADDRESS		
32-BIT DESTINATION IP ADDRESS		
(OPTIONS - IF ANY)		

FIG. 11

0015395-003005

TCP HEADER (20 BYTES)

16-BIT SOURCE PORT	16-BIT DESTINATION PORT
32-BIT SEQUENCE NUMBER	
32-BIT ACKNOWLEDGMENT NUMBER	
URG/ACK/PSH/RST/SYN/FIN	16-BIT WINDOW SIZE
16-BIT TCP CHECKSUM	16-BIT URGENT POINTER

FIG. 12

The diagram illustrates the SWIFT system architecture. At the top, three main components are connected to a **System Bus** (labeled 42):

- Host Processor** (labeled 44)
- Bus Arbitration Logic** (labeled 47)
- Shared Memory** (labeled 46)

Below the System Bus is the **SWIFT** block (labeled 40), which contains several internal components and buses:

- CPC** (labeled 92) and **DMA** (labeled 85) are connected to the **CPC Bus** (labeled 250).
- The **Interrupt Bus** (labeled 252) is shown below the CPC Bus.
- The **FIFO Bus** (labeled 254) is shown below the Interrupt Bus.
- At the bottom of the SWIFT block, there are five vertical components:
 - Three individual components labeled 50, 52, and 54.
 - A larger component labeled 56 containing two sub-components: **Tx FIFO** (labeled 70) and **Rx FIFO** (labeled 72).
- Each of these five components is connected to a set of three vertical lines at the very bottom of the diagram, representing external interfaces or connections.

FIG. 13

[illegible]

Rx Threshold Reached – Start-Of-Packet Interrupt Sent to CPC

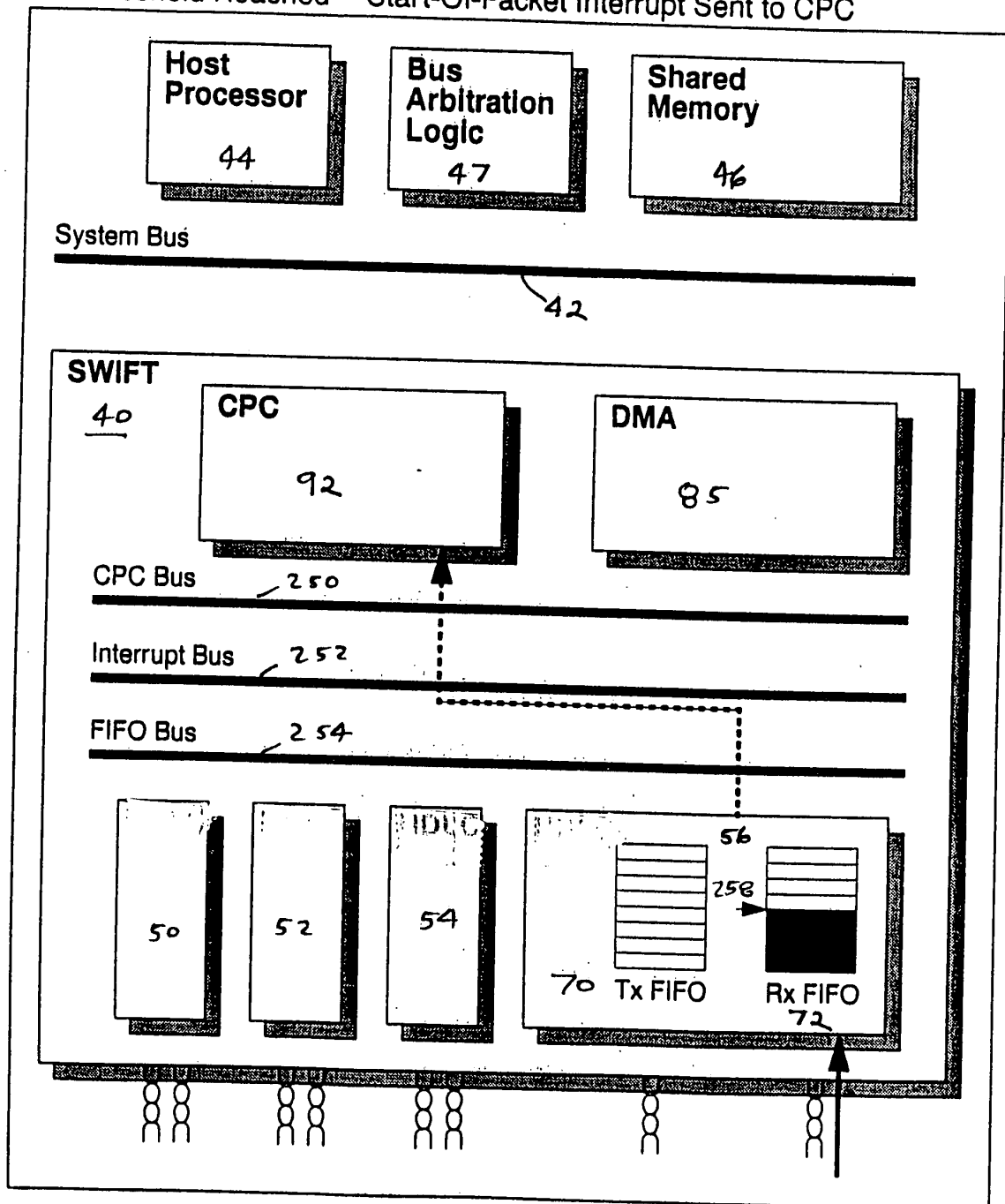


FIG. 15

CPC Issues a Command to DMA to Transfer Data

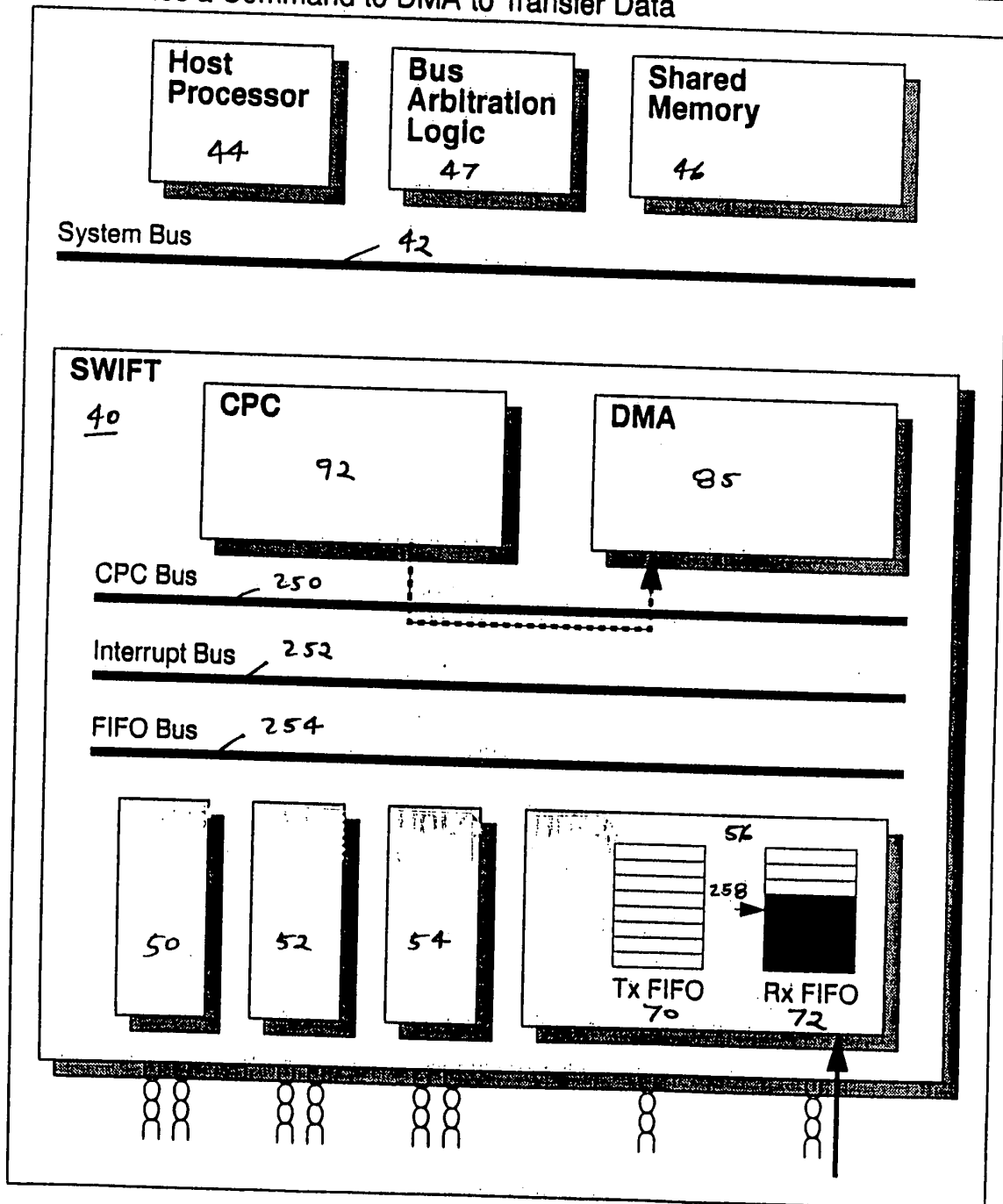


FIG. 16

DMA Negotiates for Ownership of System Bus

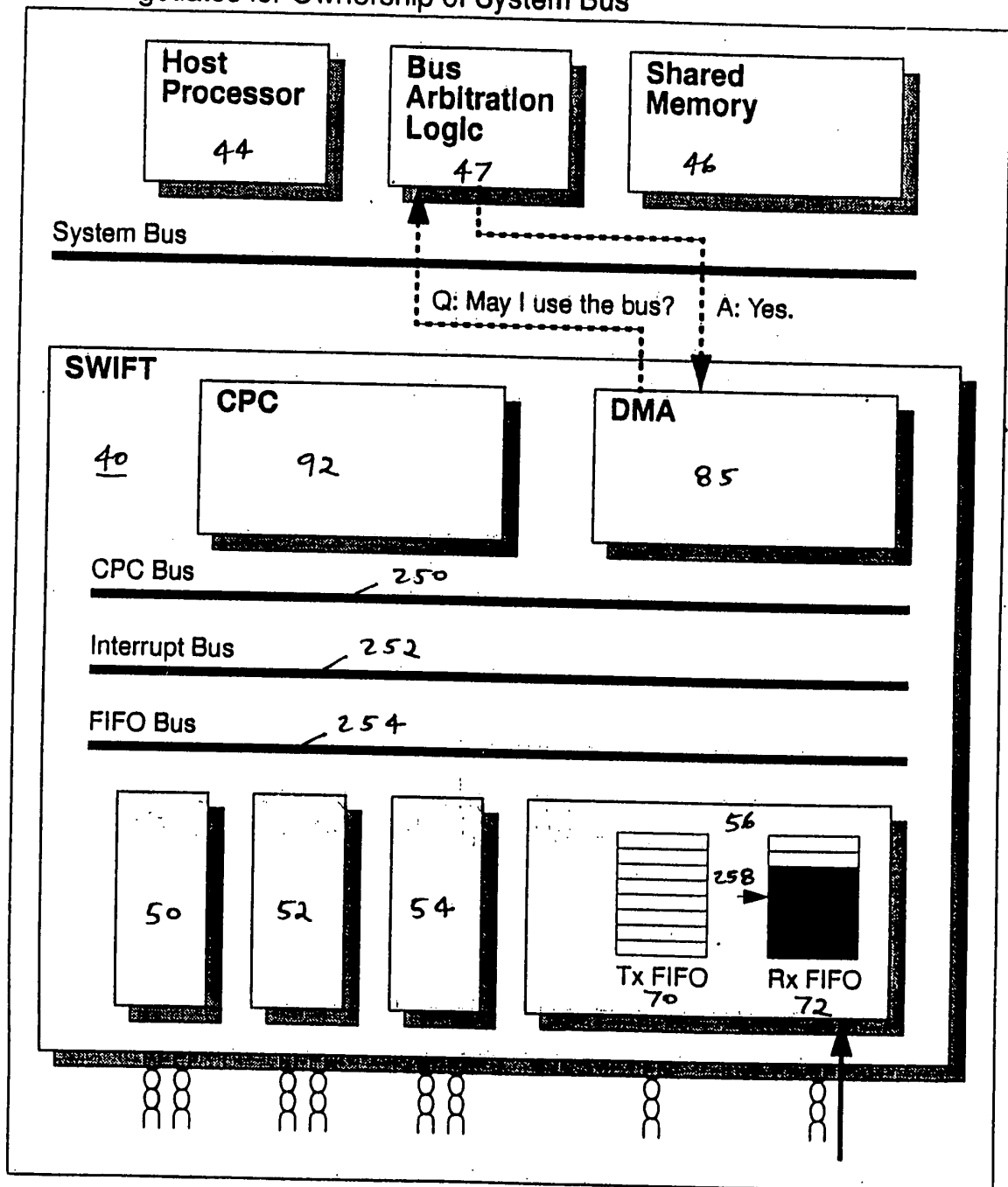


FIG. 17

DMA Transfers Data from Rx FIFO to Shared System Memory

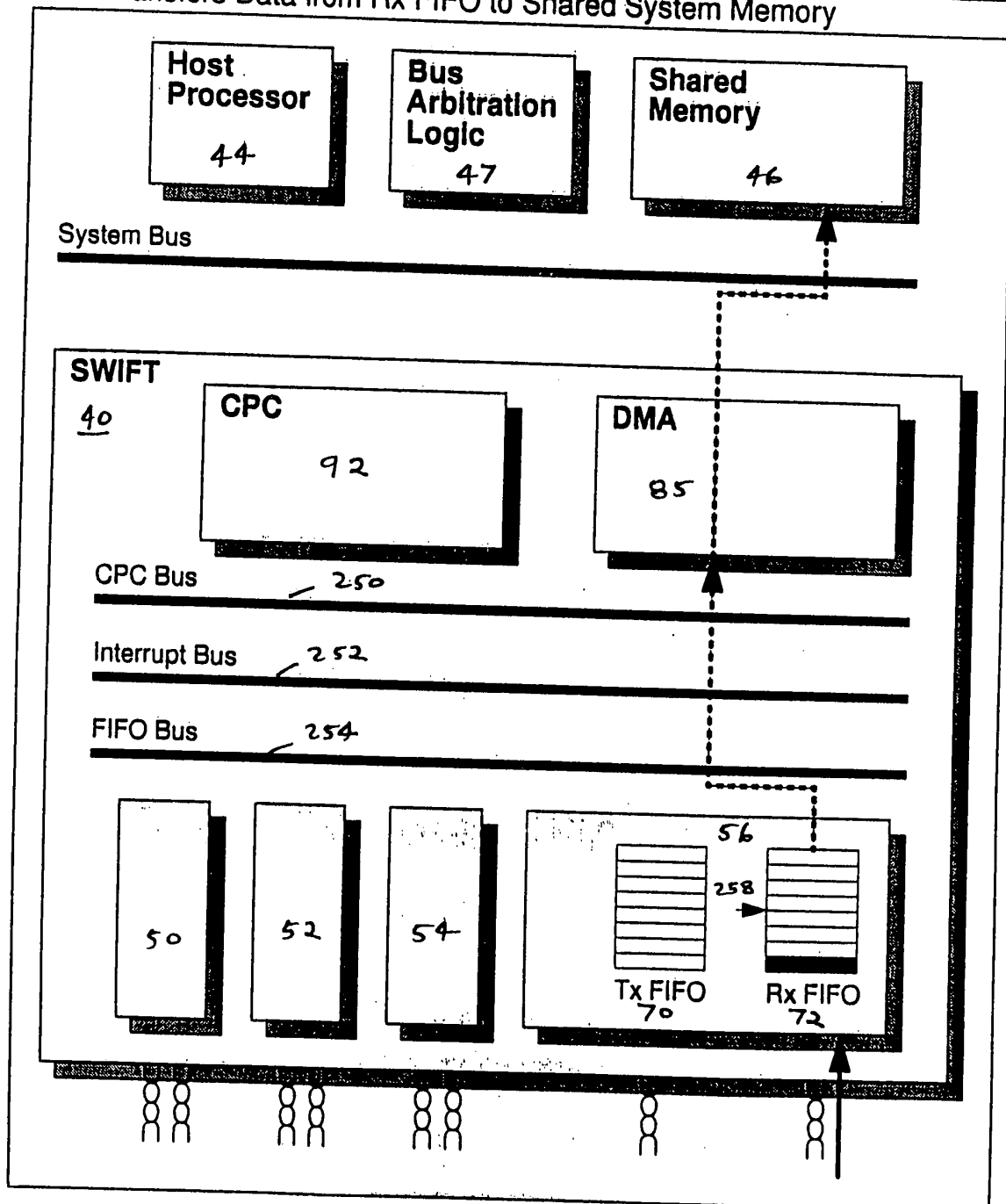


FIG. 18

60260-5029160

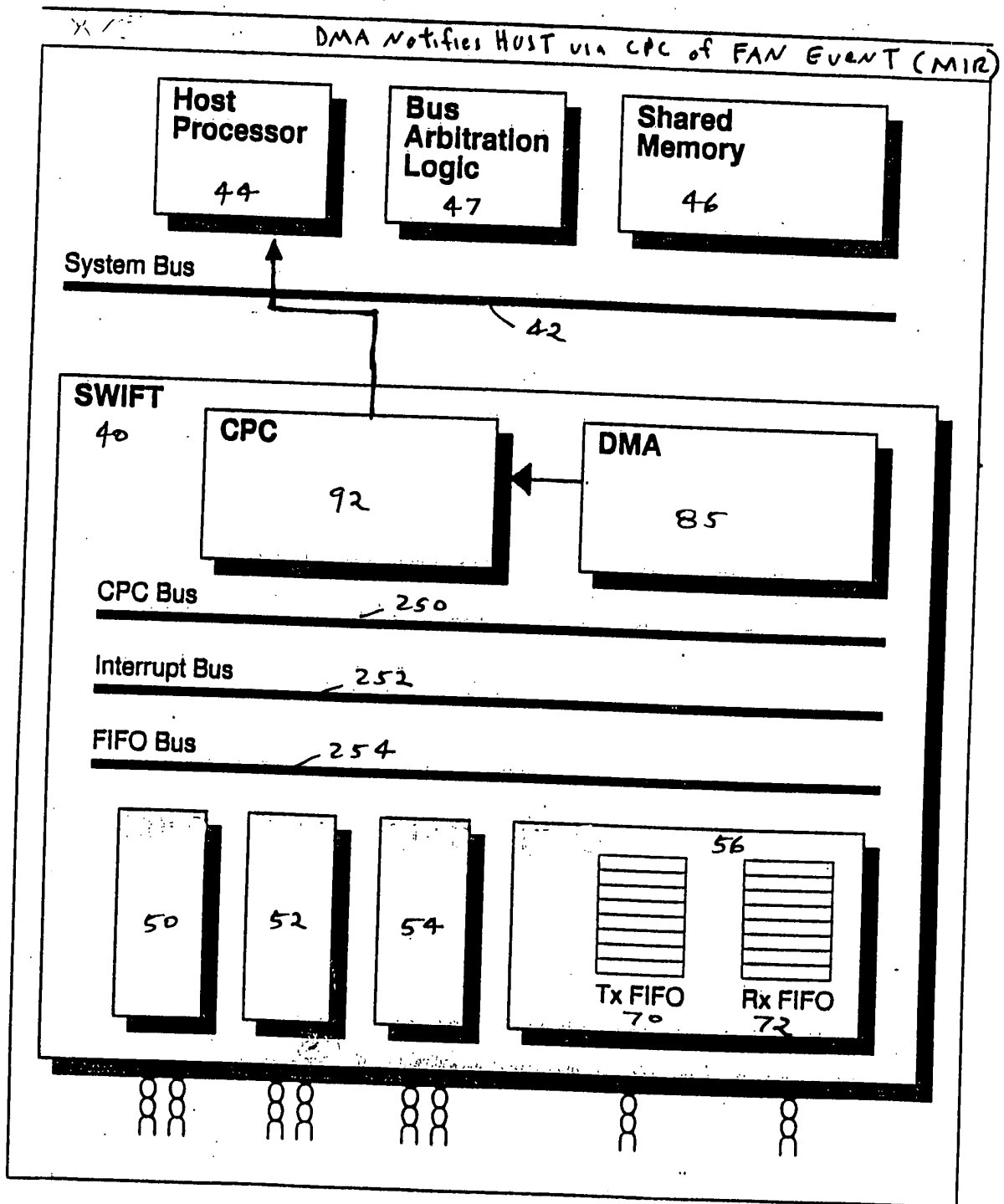


FIG. 19

000005269540

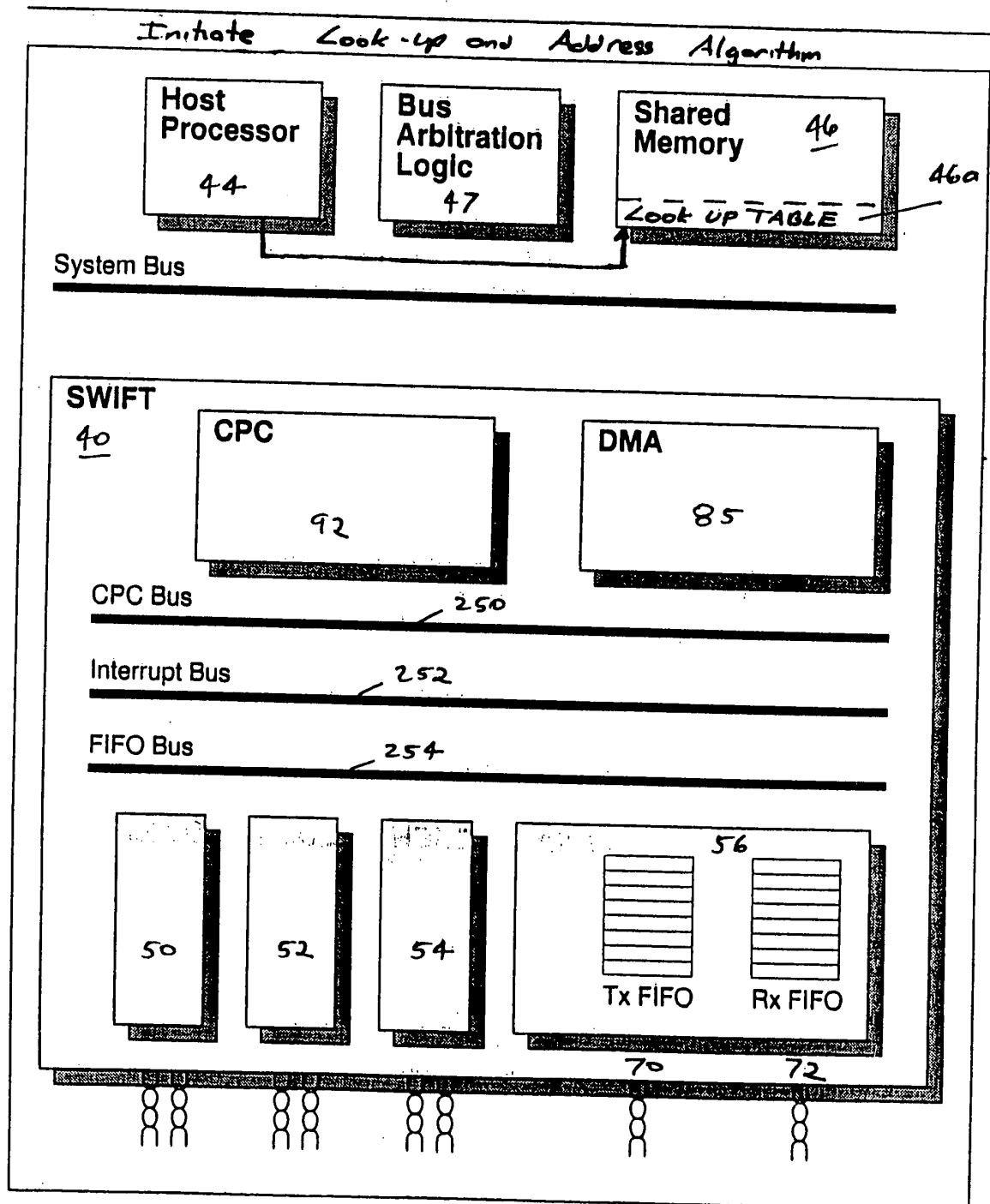


FIG. 20

60000-50000

FRAME ADDRESS NOTIFICATION (FAN)

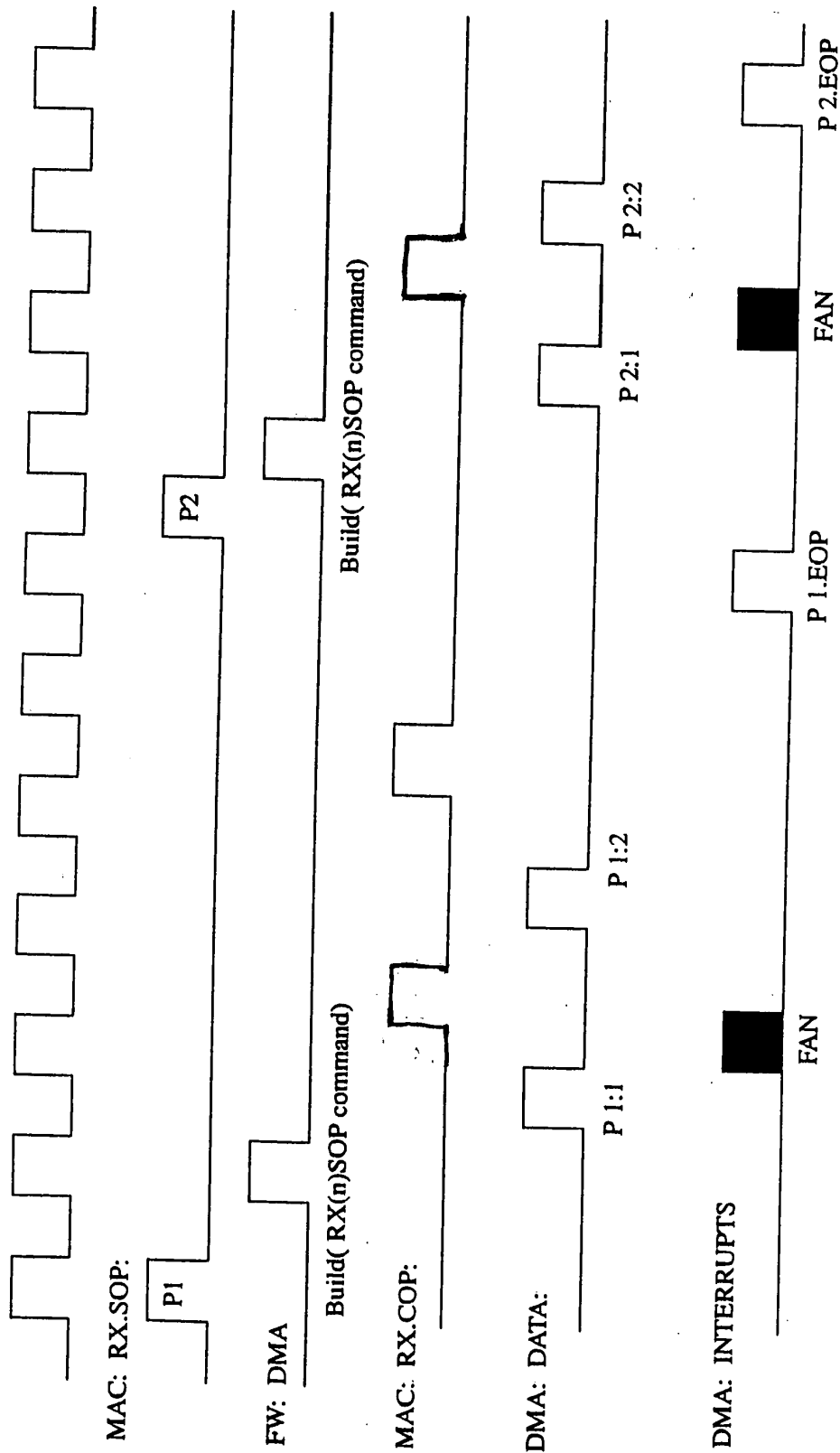


FIG. 21

600260-522500

CONVENTIONAL FIFO FLOW-CONTROL VERSUS LAWM

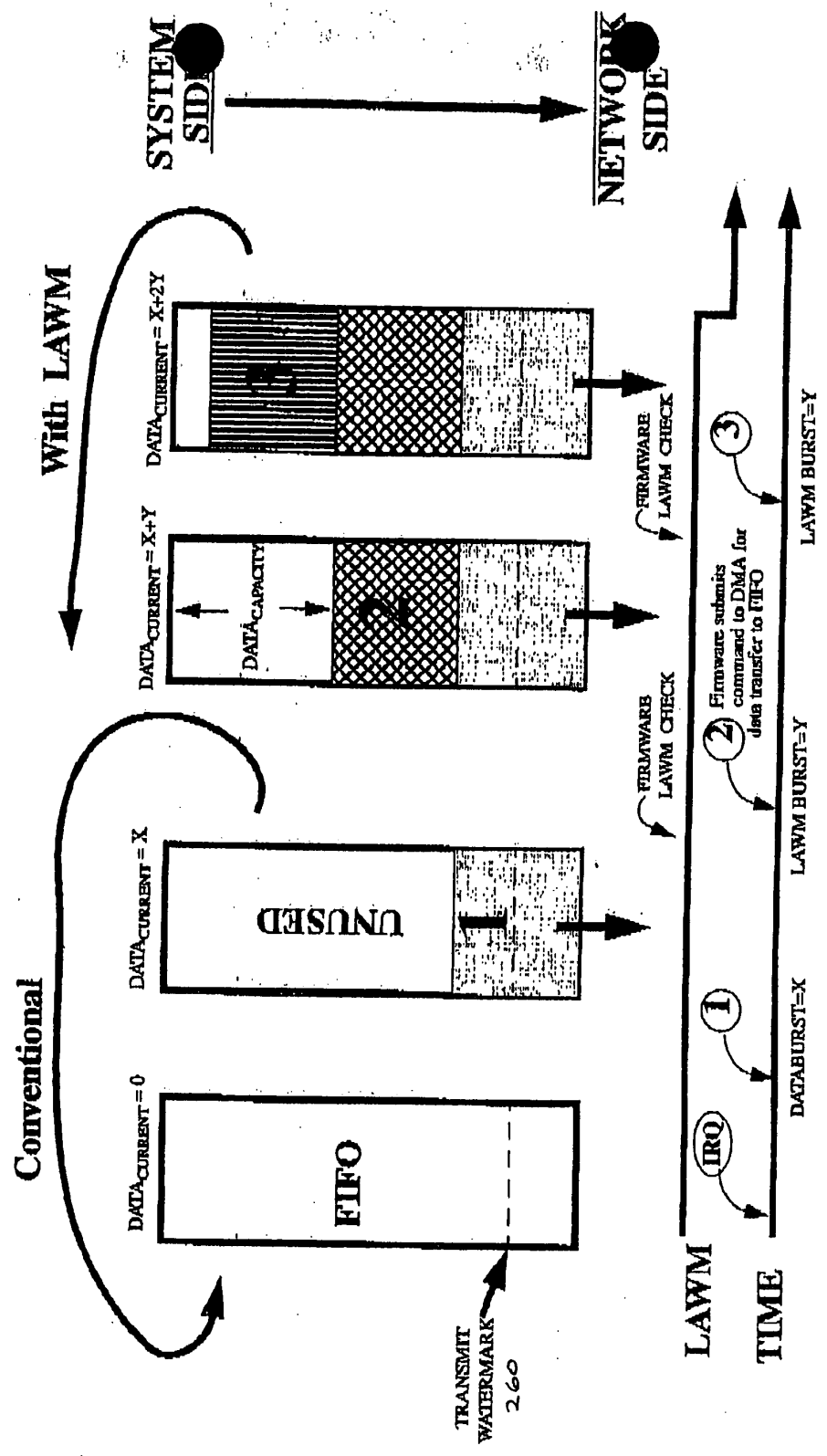


Fig. 22

00453000:002000

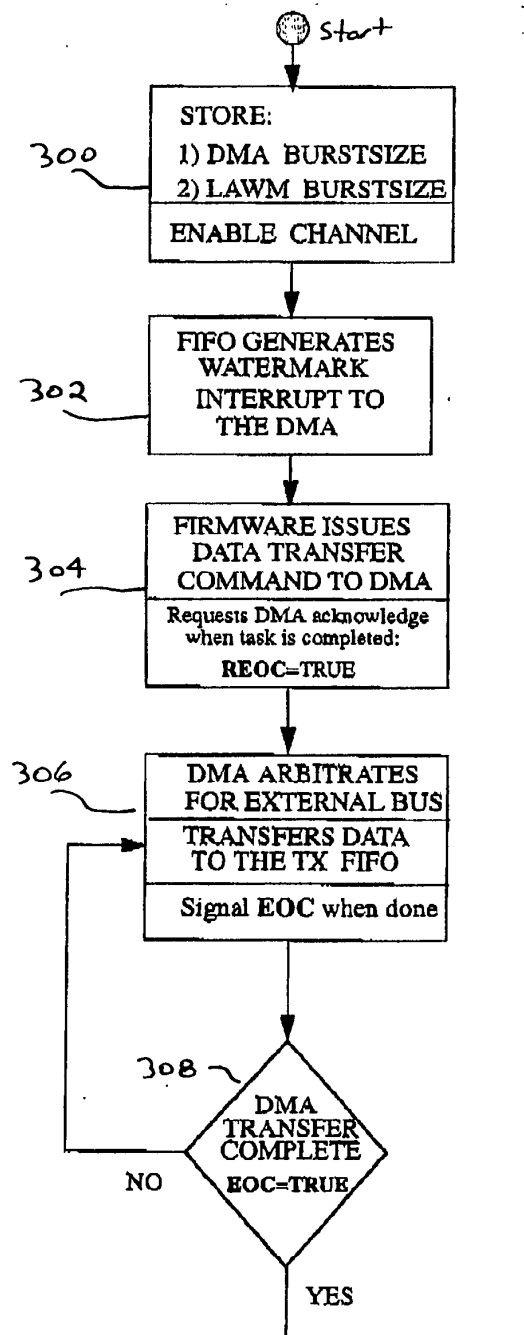
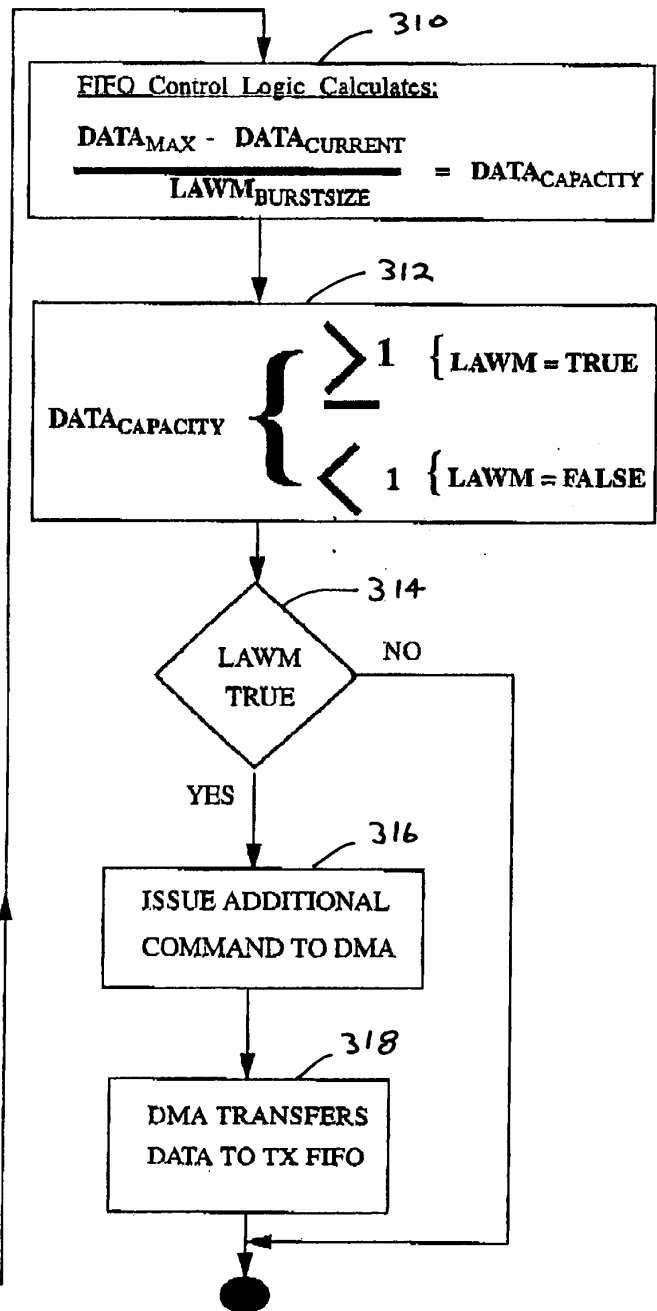


Fig. 23



600200-500250

INTERRUPT-MEDIATED FRAME TRANSMISSION

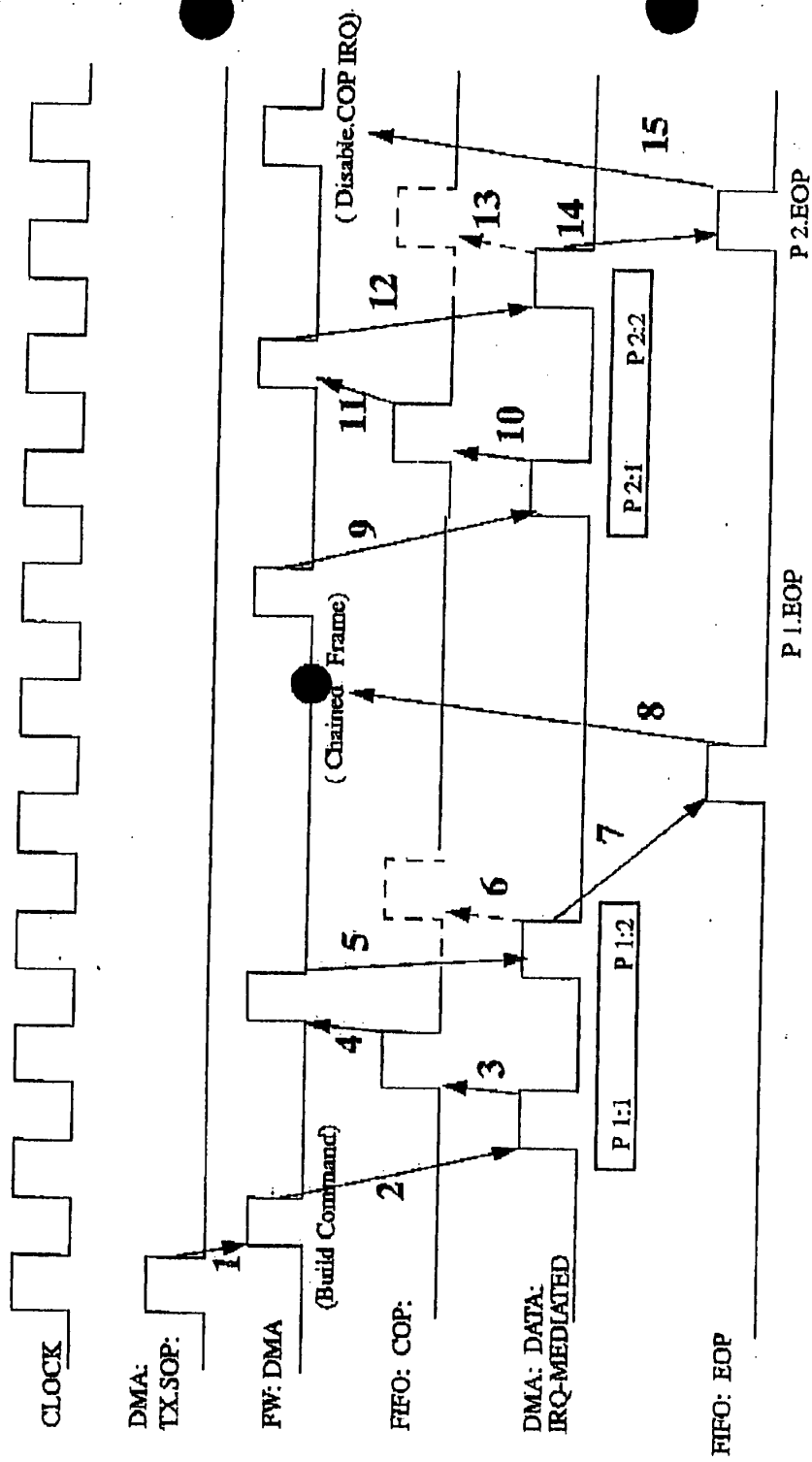


FIG. 24a

66000-560500

LAWM-MEDIATED FRAME TRANSMISSION

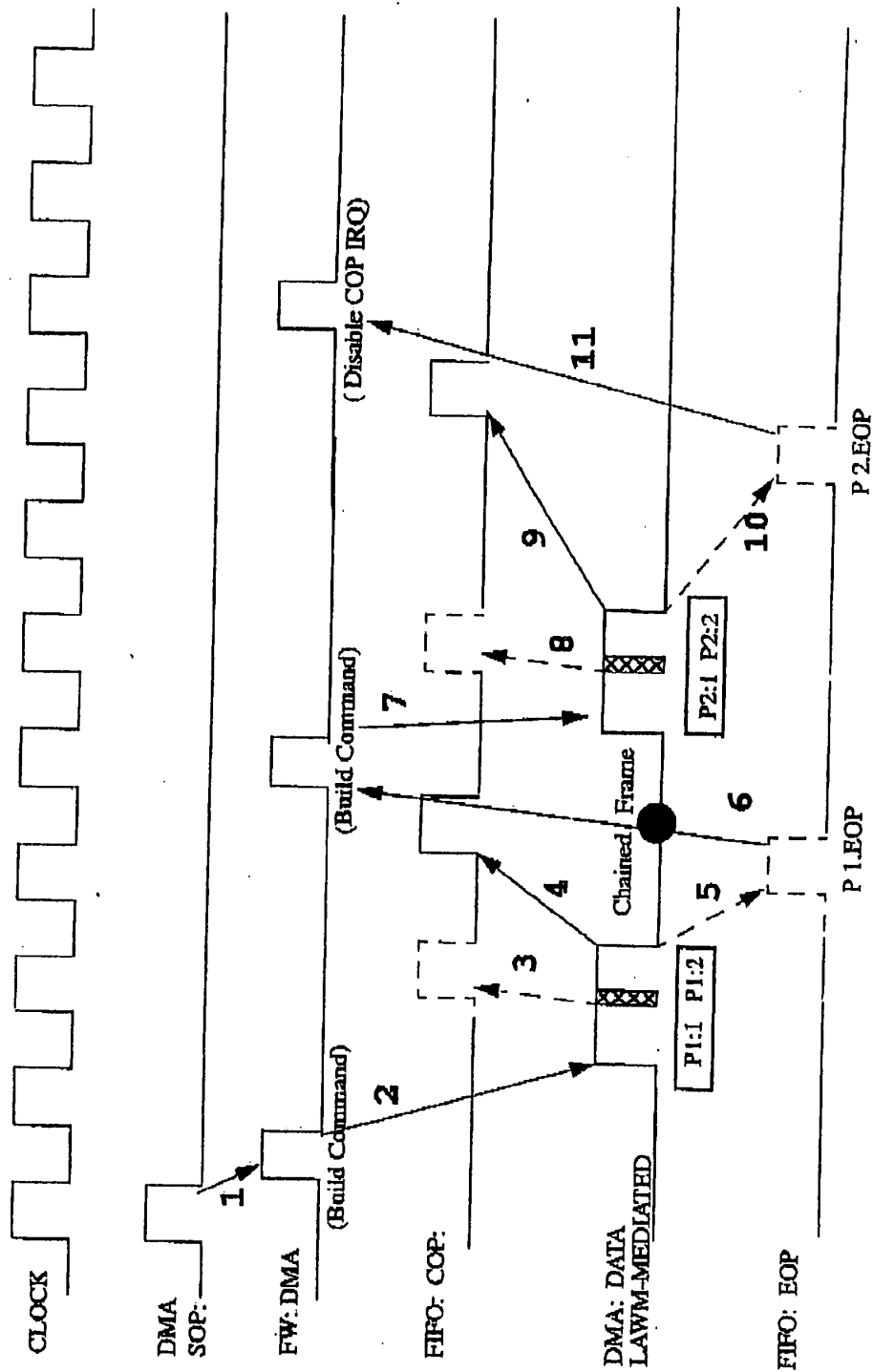
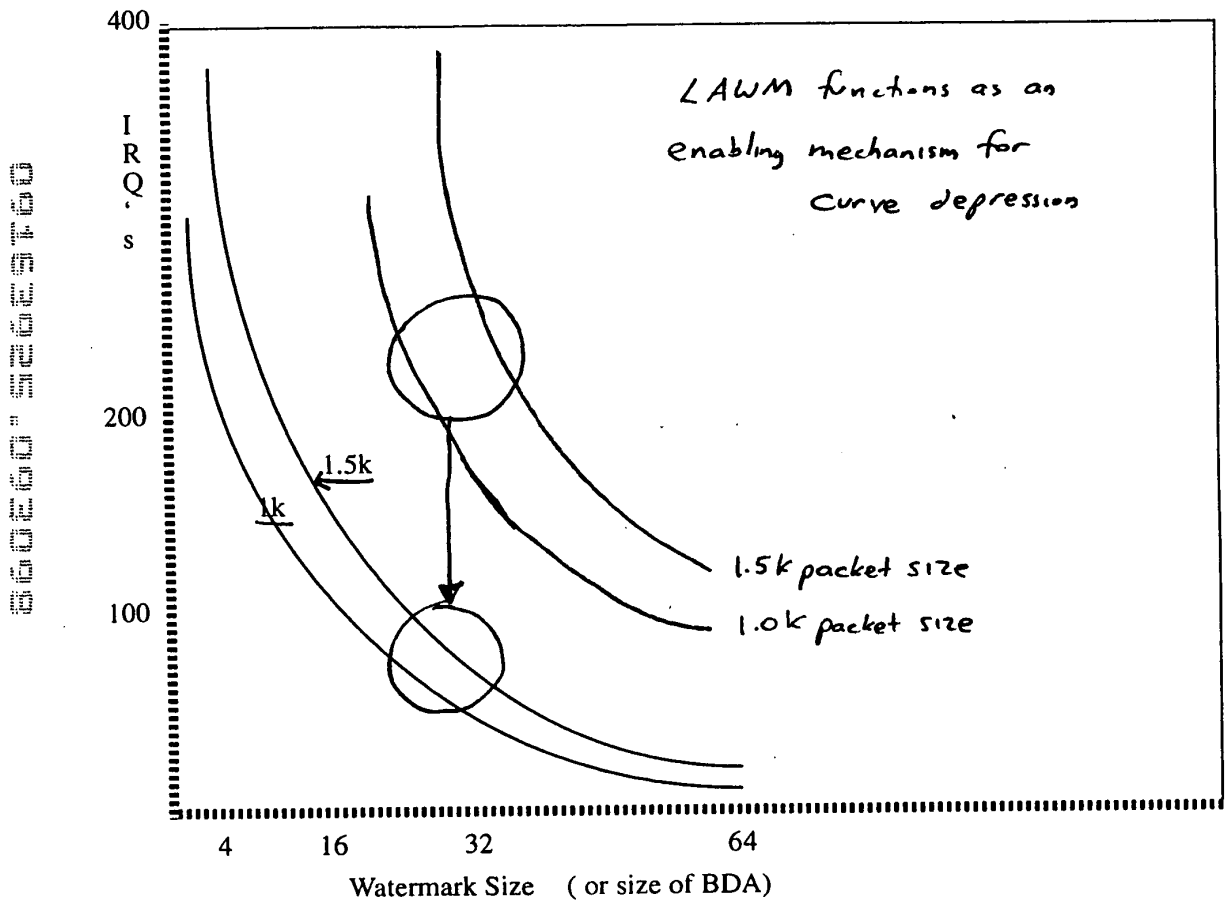


FIG. 24b

FIG. 25

Watermark effects on IRQ generation with regard to packet size:



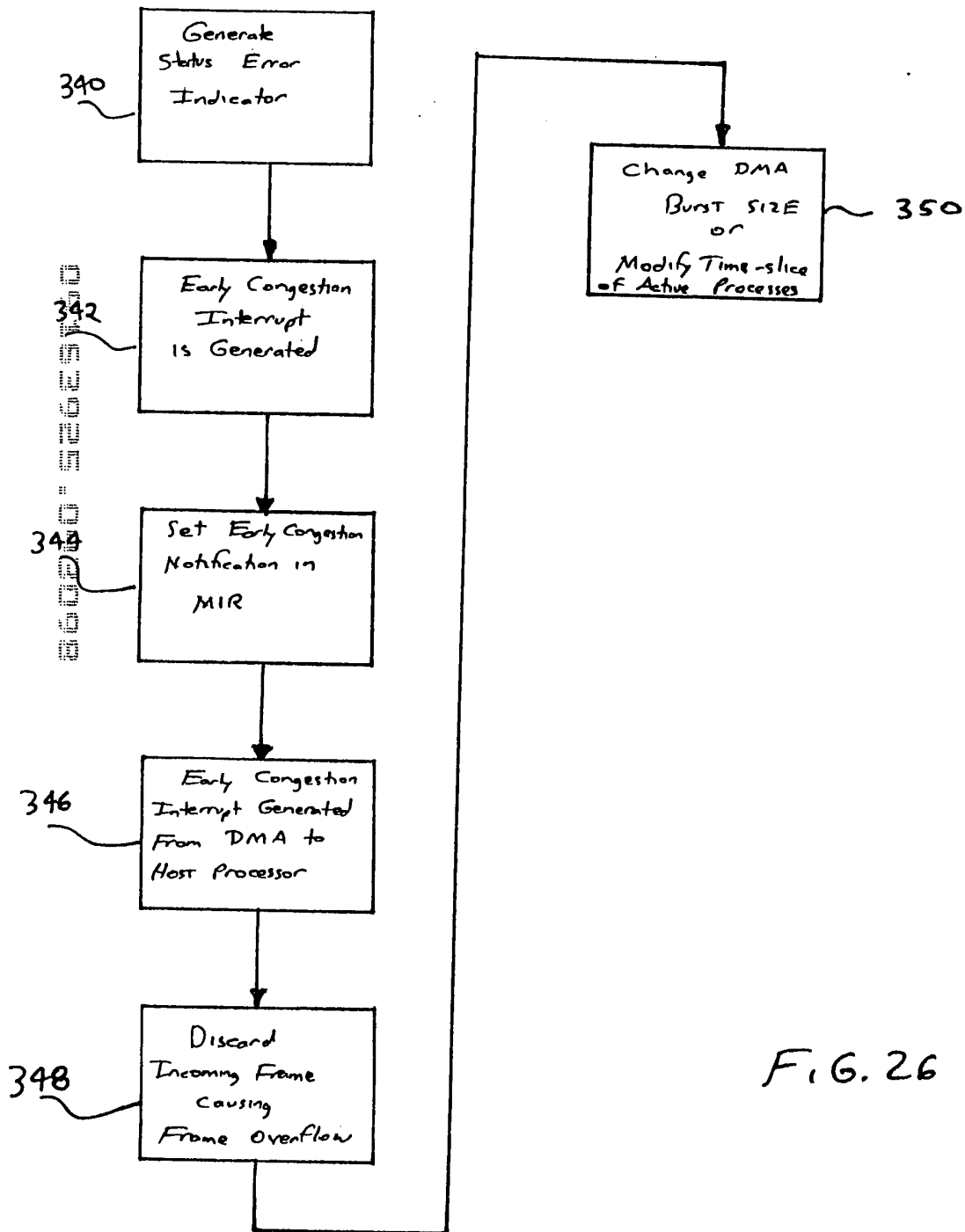


FIG. 26

FIFO Cases Overflow on Second Packet into Receive Fifo

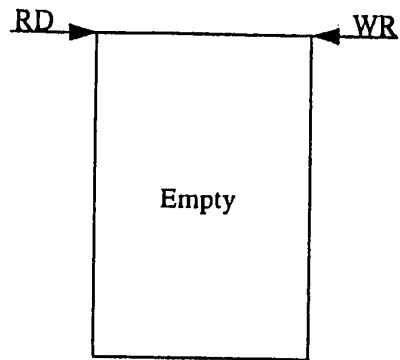


FIG. 27a

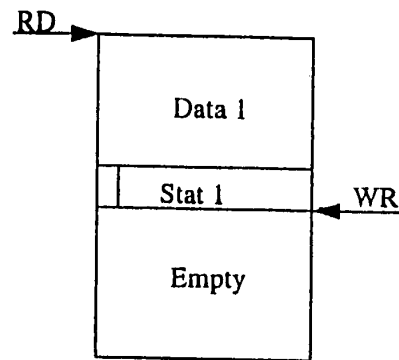


FIG. 27b

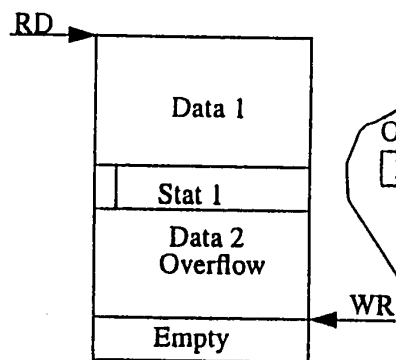


Fig. 27c

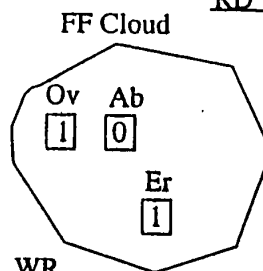


Fig. 27g

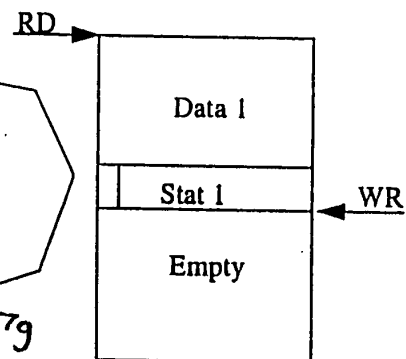


FIG. 27d

Write Pointer Reset to Beginning of Packet 2
Frozen until EOP Occurs at Which Time
Error Status for Overflow Packet is Entered.

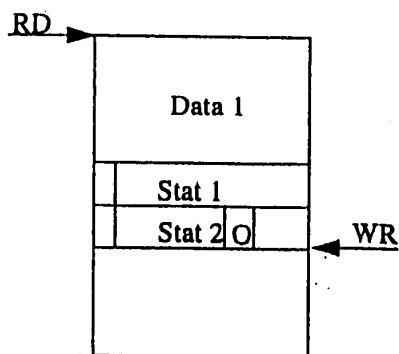
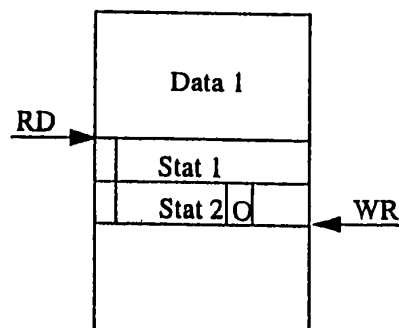


Fig. 27e



Read of Stat 1 by DMA copies it into Receive
Status Register at Host Address. No
requests to DMA for another data transfer will
occur until CPC reads status. This prevents
overwriting of status register by overflow status.

FIG. 27f

Rx FIFO Begins to Fill with a New Packet

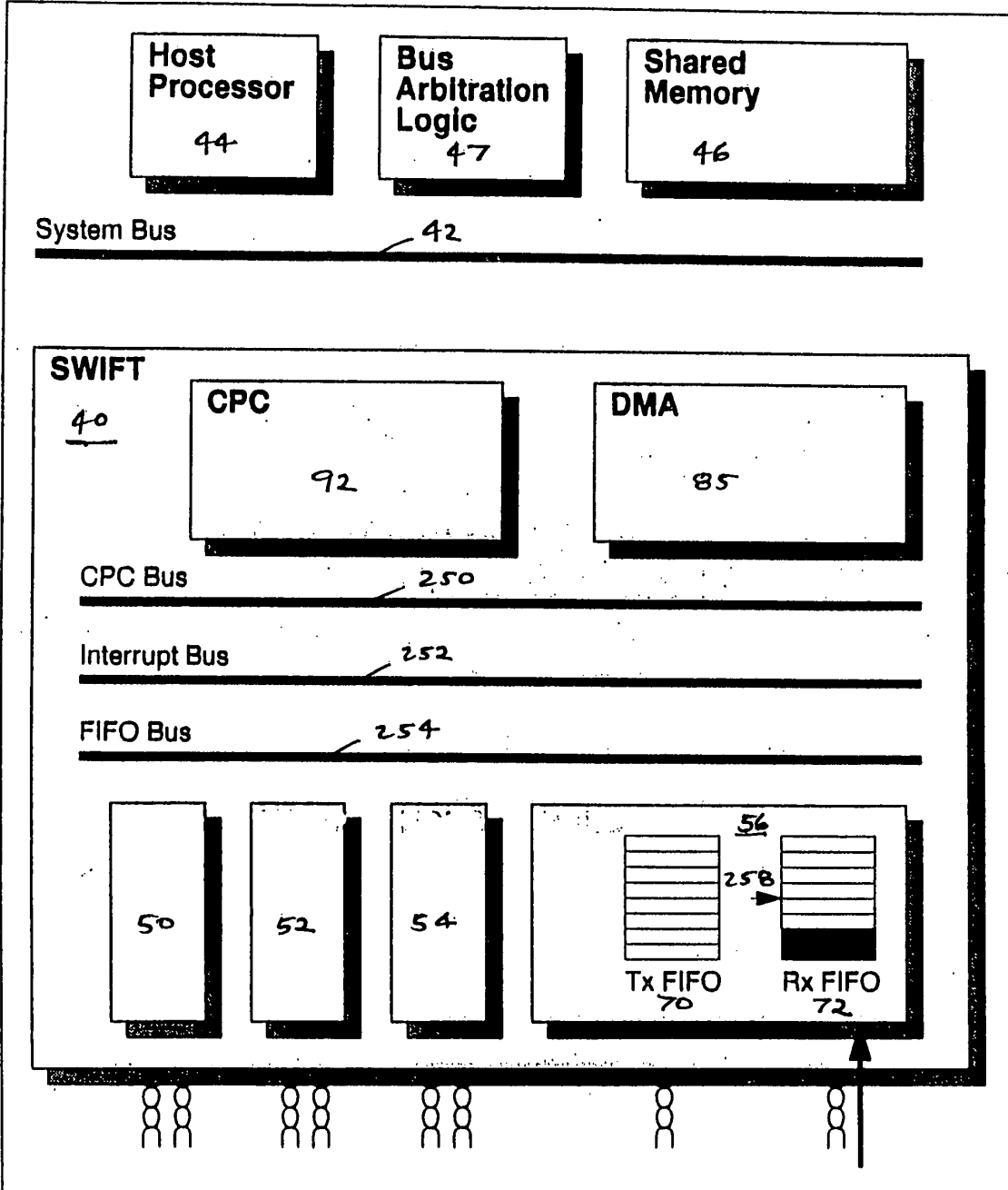


FIG. 29

Rx Threshold Reached – Start-Of-Packet Interrupt Sent to CPC

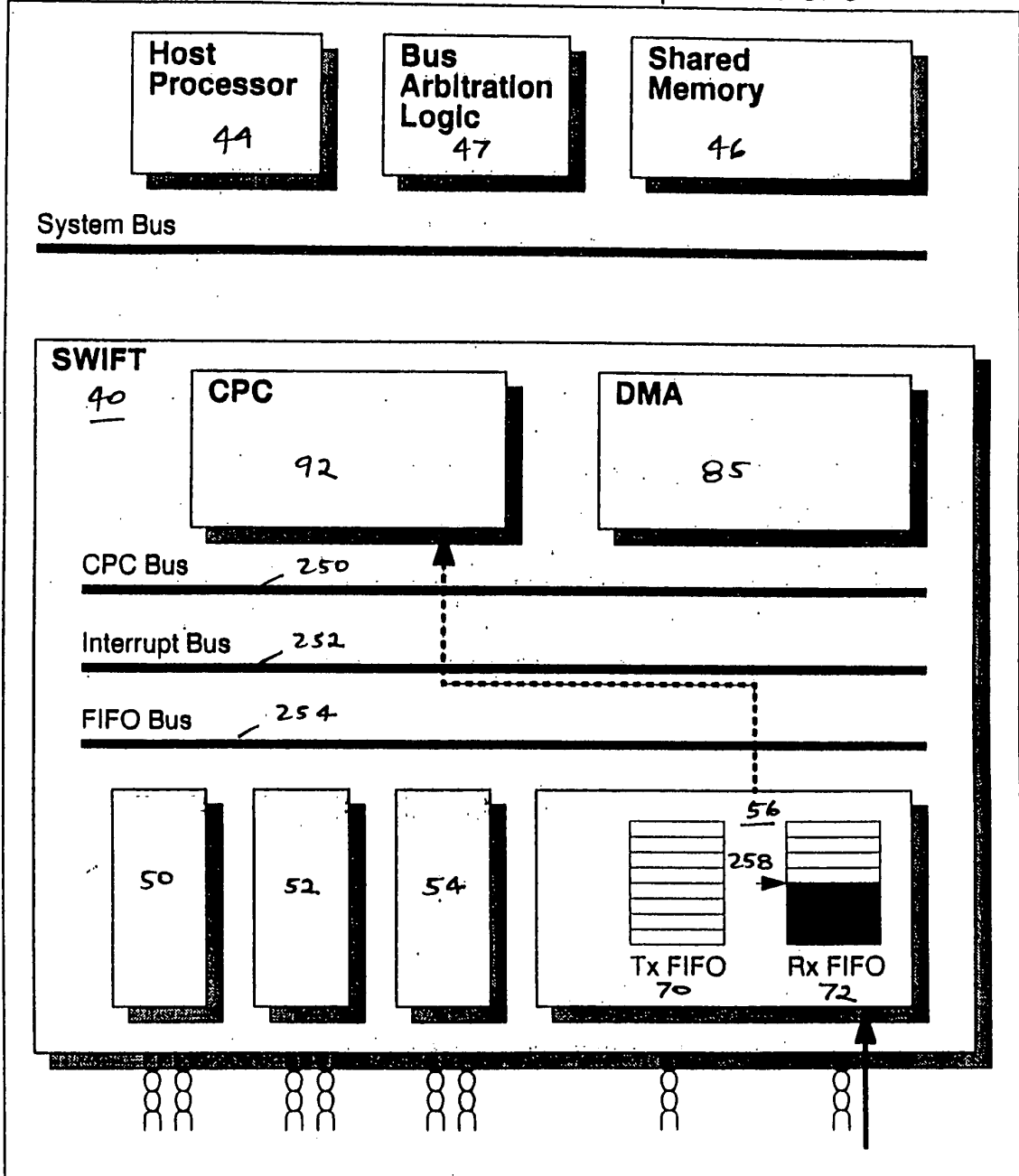


FIG. 30

CPC Issues a Command to DMA to Transfer Data

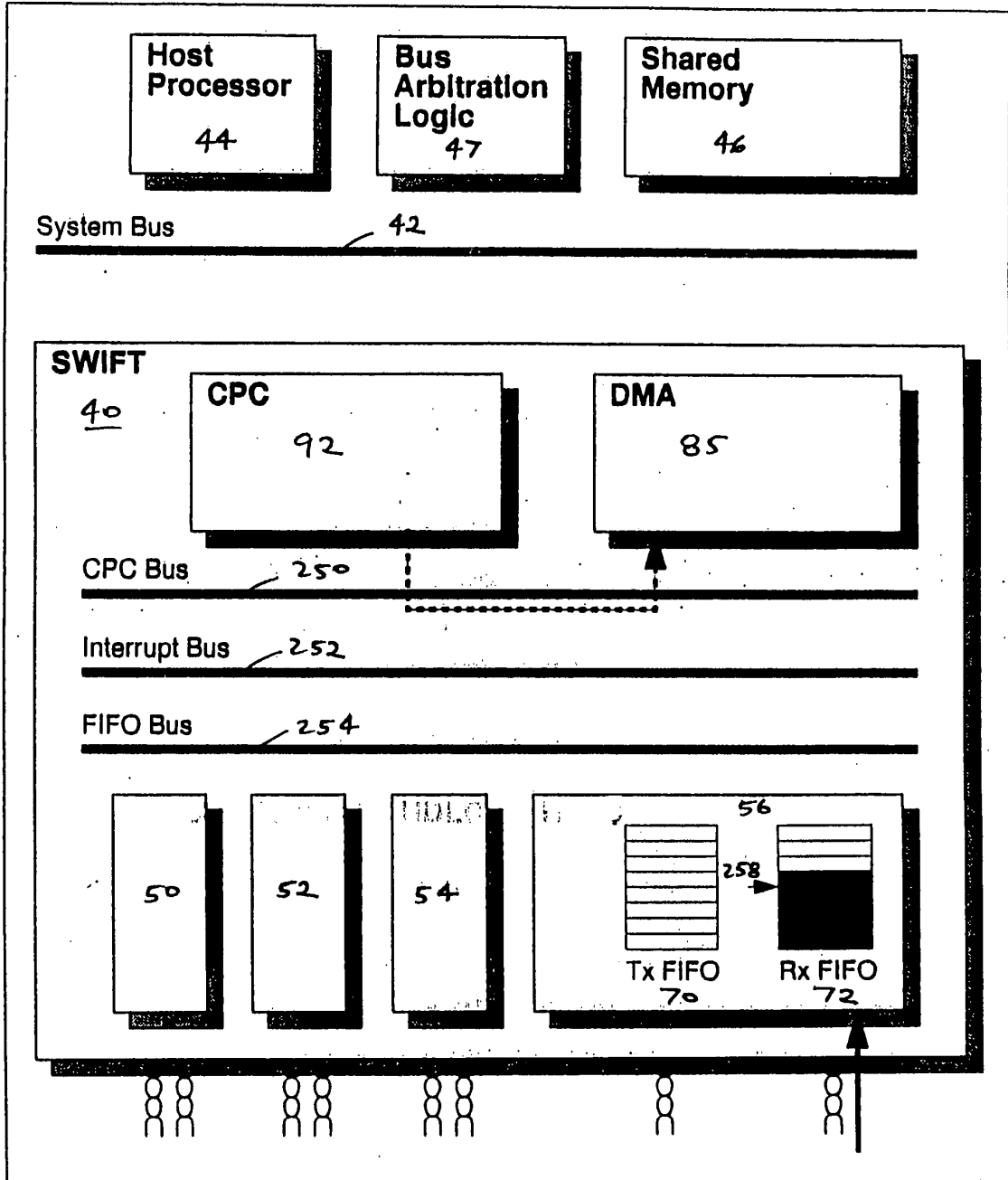


FIG. 31

[illegible]

DMA Transfers Data from Rx FIFO to Shared System Memory

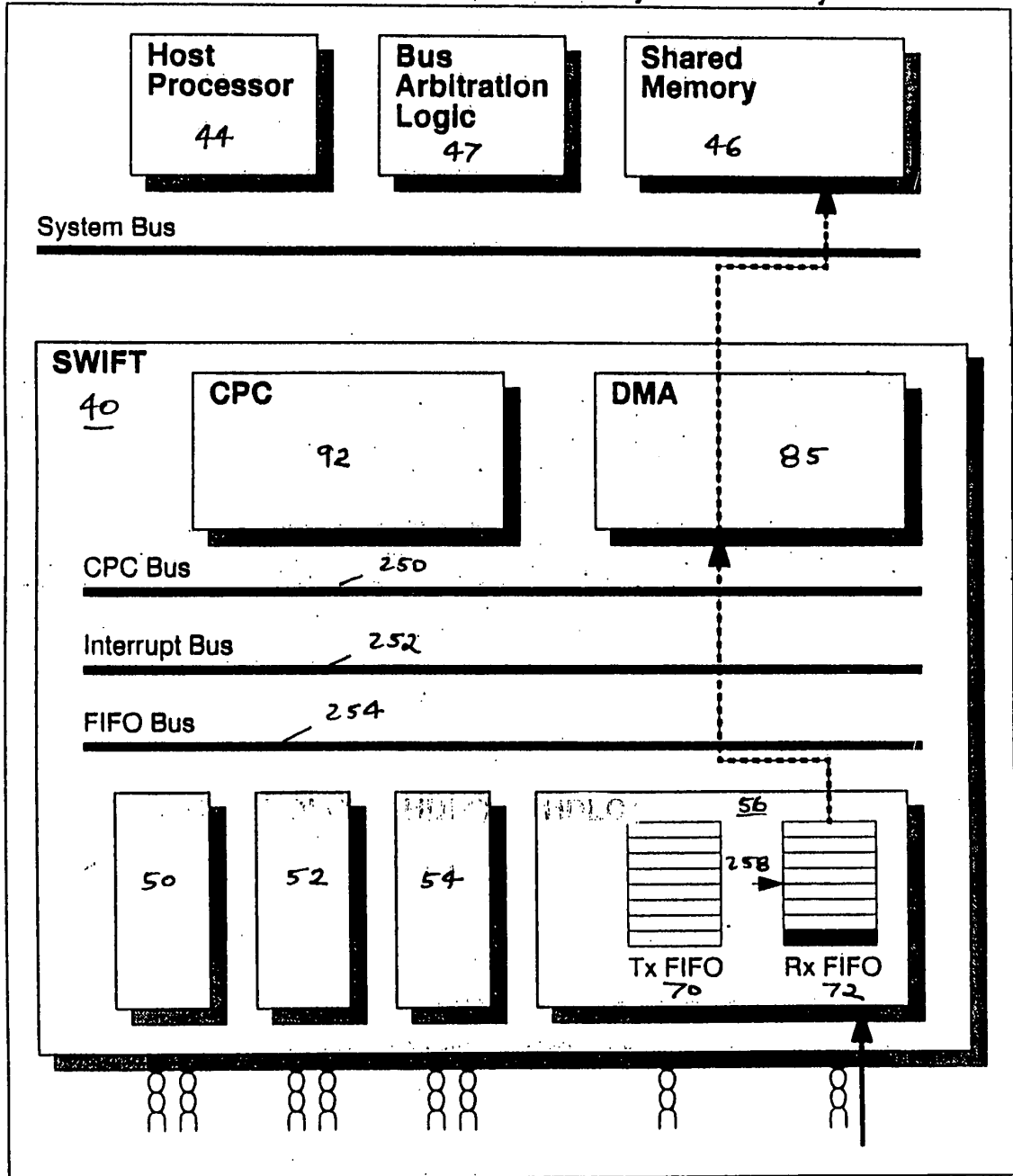


FIG. 33

Rx FIFO Begins to Fill with a New Packet 2

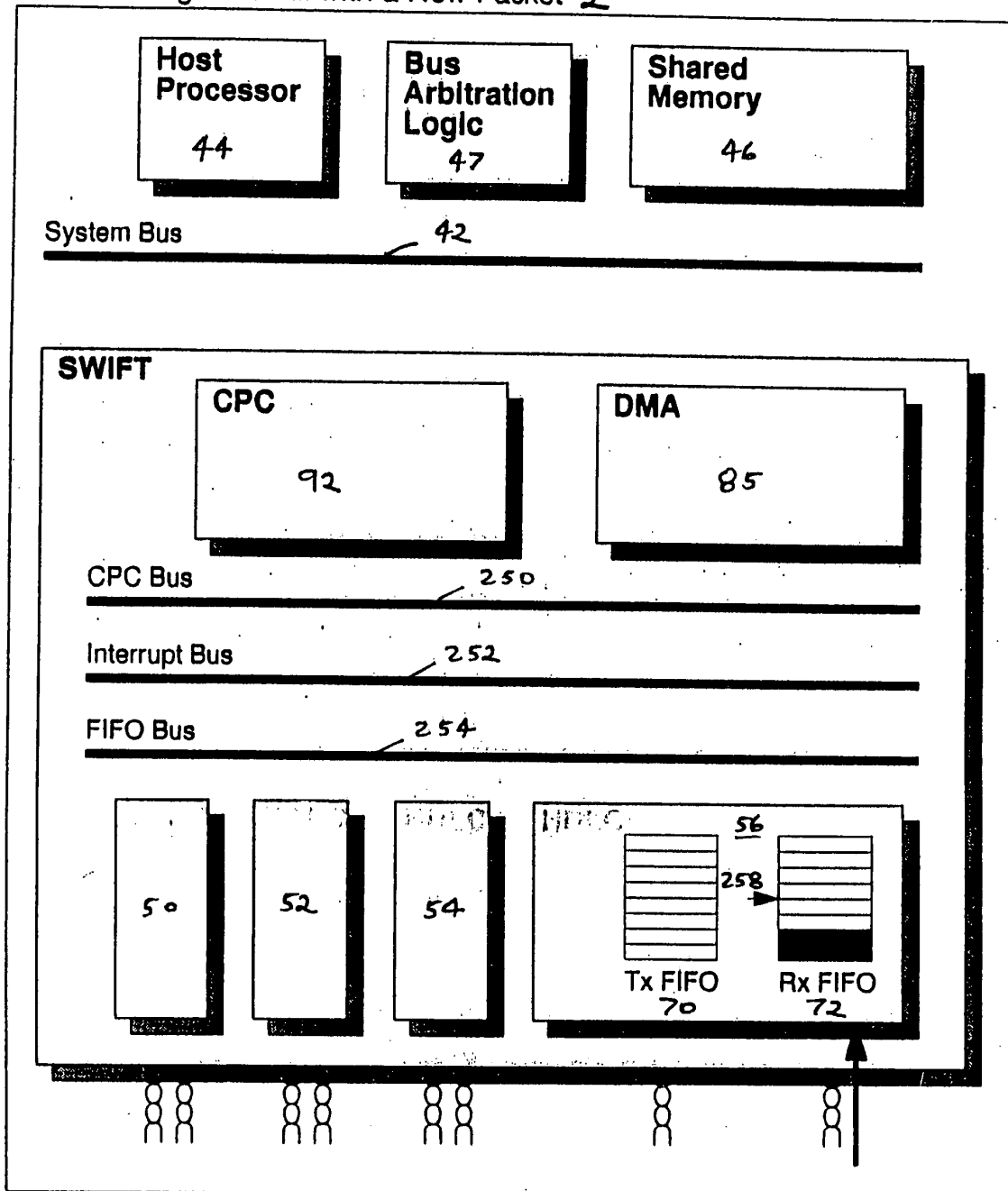


FIG. 34

Rx Threshold Reached – Start-Of-Packet Interrupt Sent to CPC

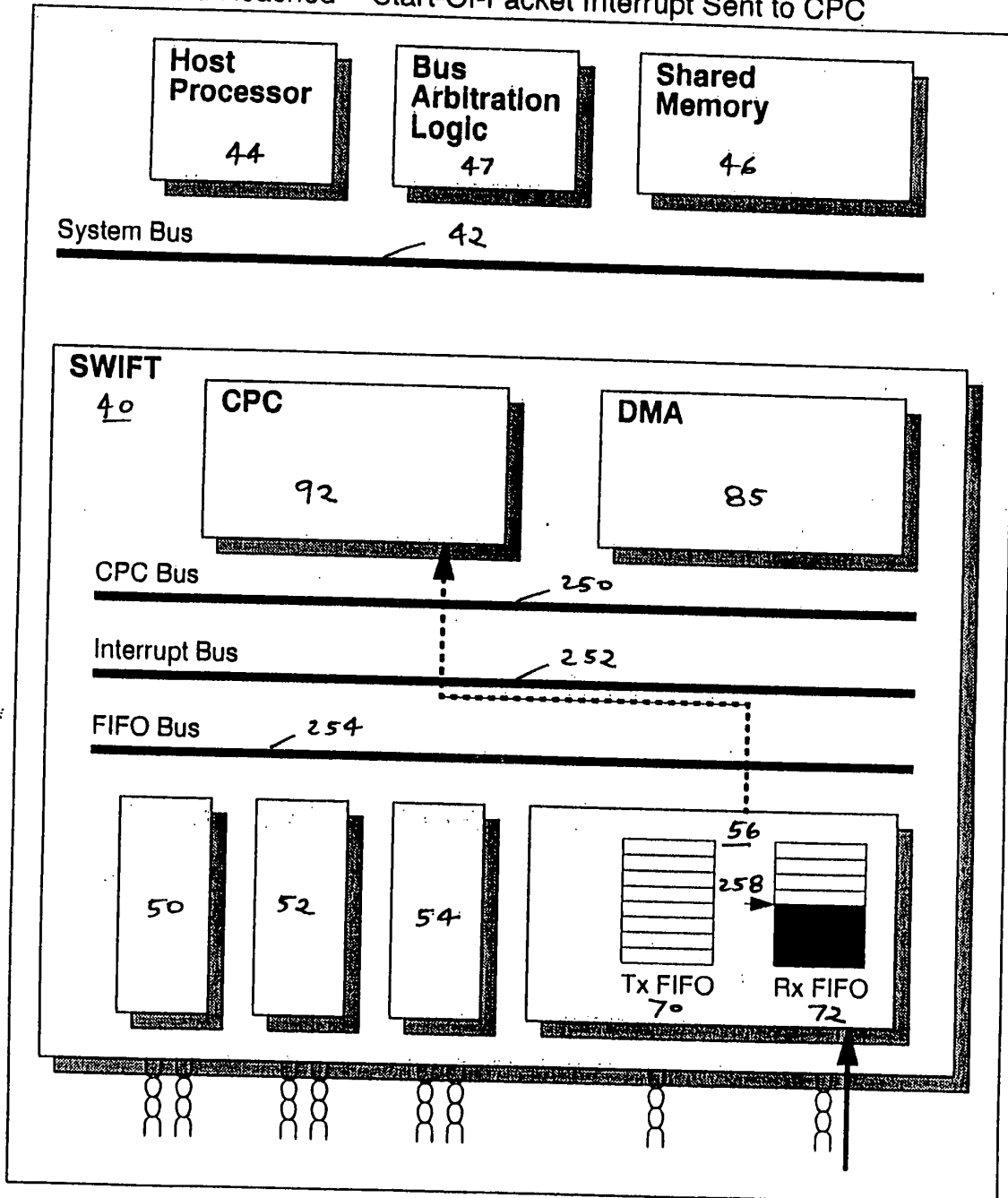
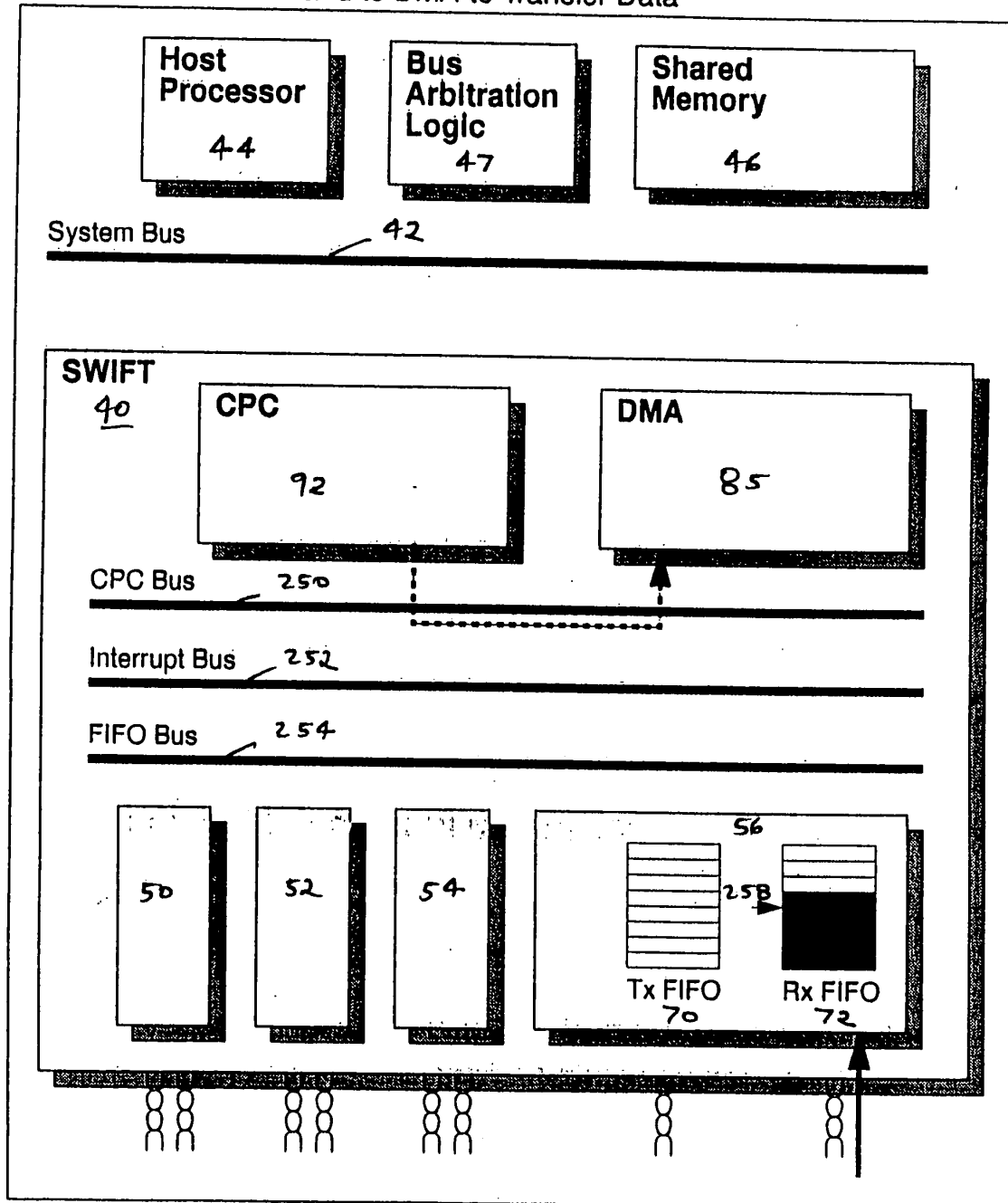


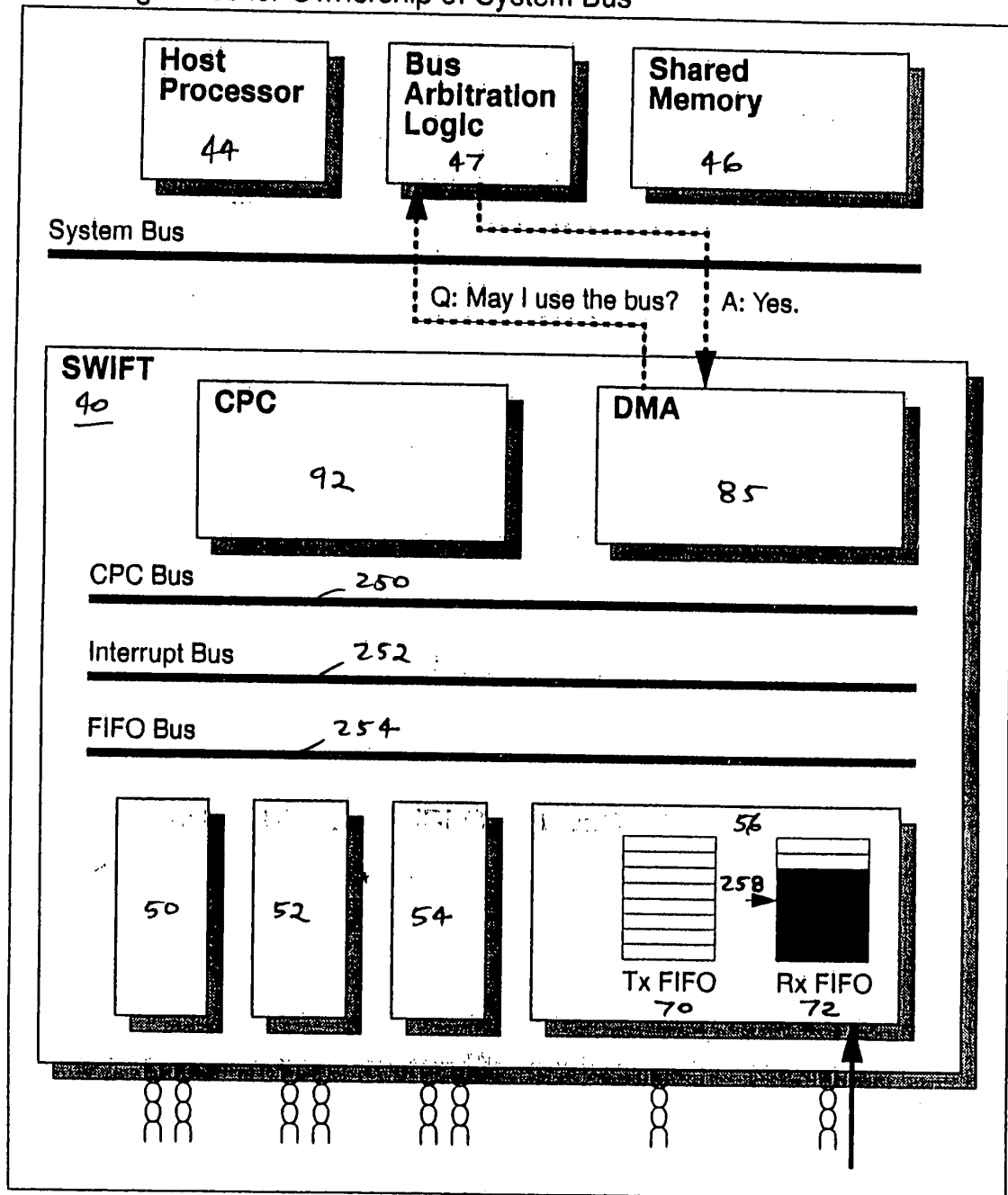
FIG. 35

CPC Issues a Command to DMA to Transfer Data



F.G. 36

DMA Negotiates for Ownership of System Bus



F.6.37

001592-9265100

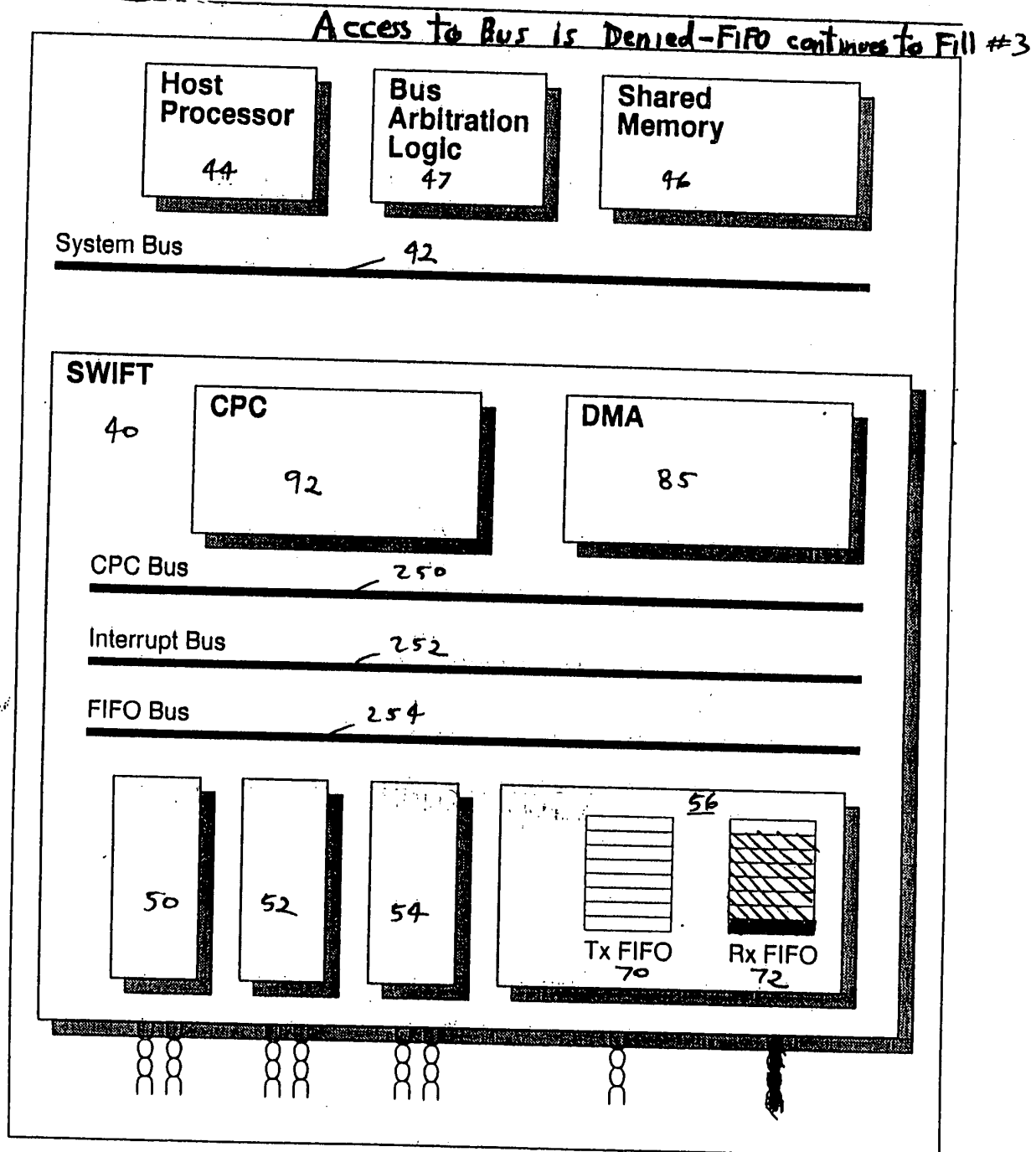


FIG. 38

Incoming Frame Overflows Rx FIFO

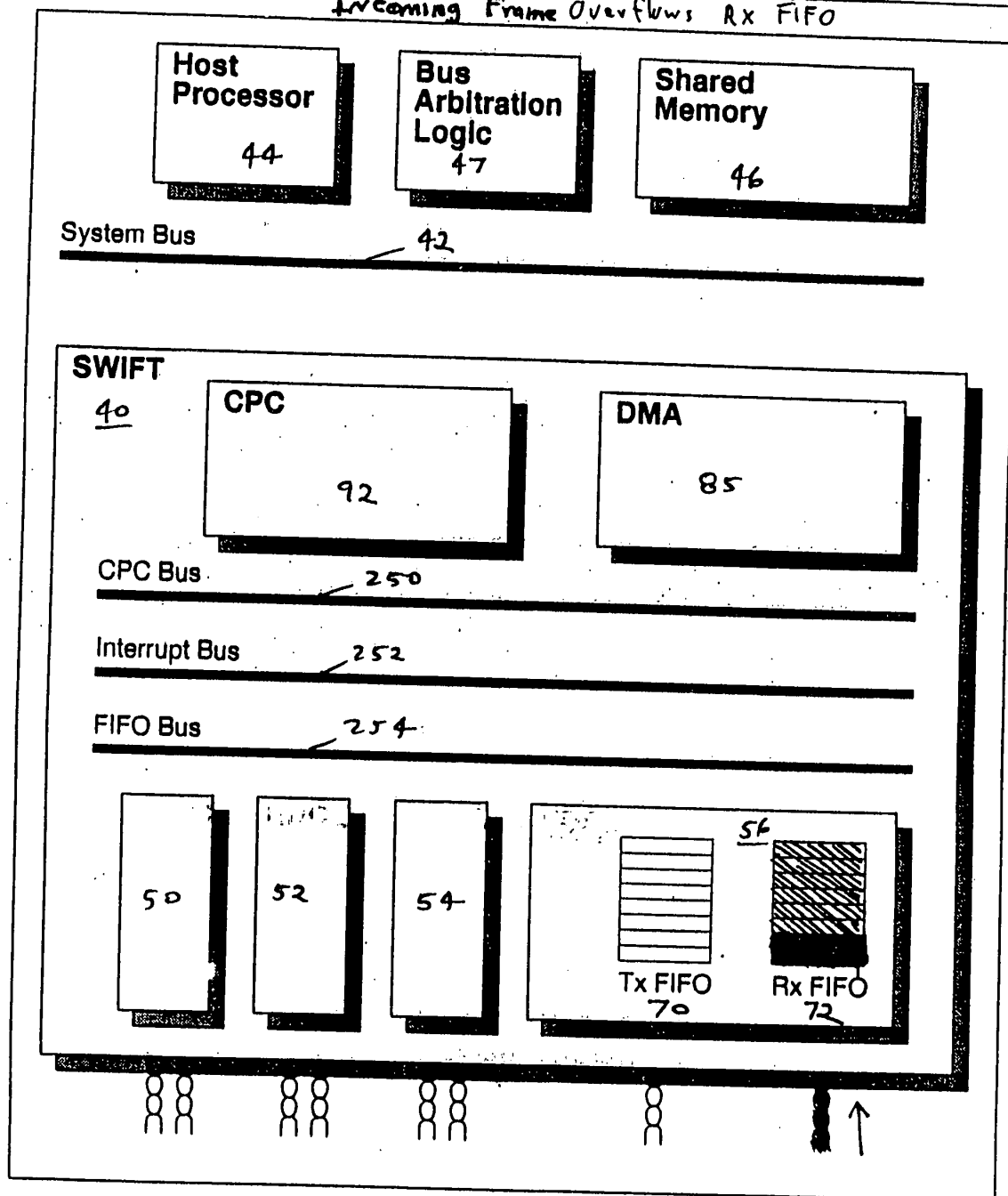
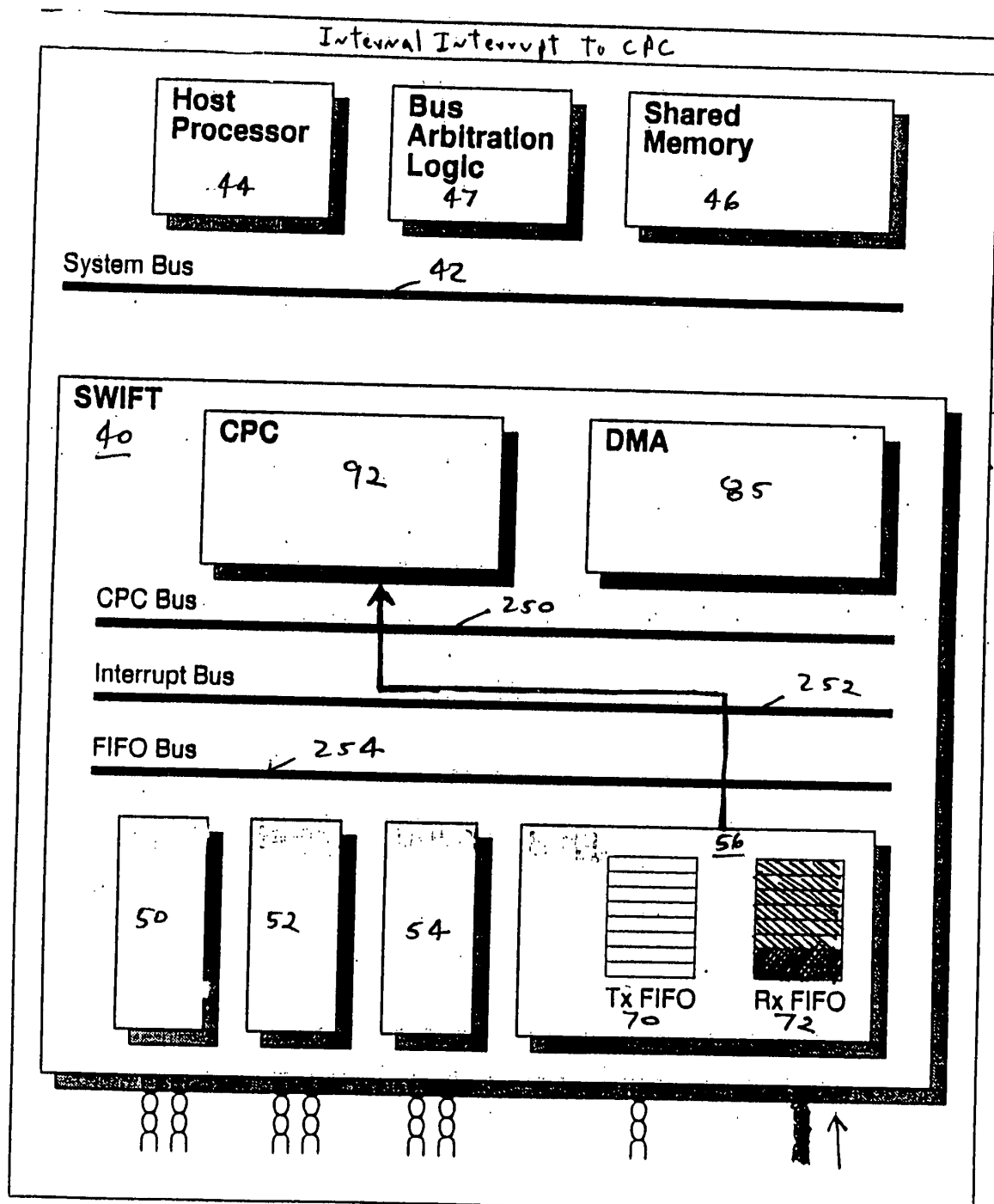


FIG. 39

56000-5625160



F. G. 40

00163035-00209
500260-50025160

Initial Block Diagram: cpc sets ECN bits for Port in Register Block of DM

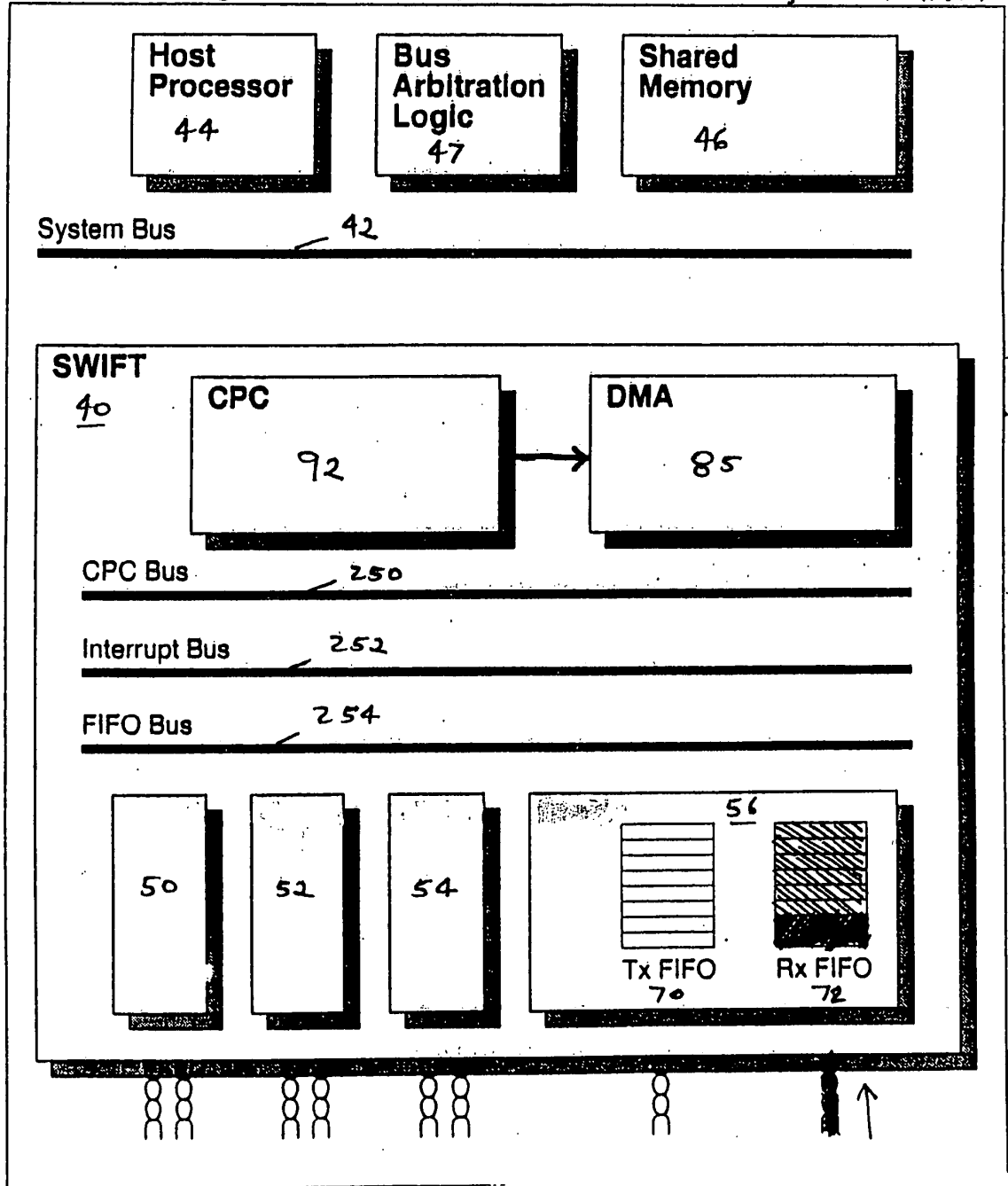


FIG. 41

The diagram illustrates the SWIFT system architecture. At the top, a horizontal line represents the **System Bus**. Above this bus are three main components: the **Host Processor 44**, **Bus Arbitration Logic 47**, and **Shared Memory 46**. Below the System Bus is a large rectangular block labeled **SWIFT 40**. Inside the SWIFT block, there are two main components: **CPC 92** and **DMA 85**. Below these are three horizontal buses: **CPC Bus 250**, **Interrupt Bus 252**, and **FIFO Bus 254**. At the bottom of the SWIFT block, there are five vertical components: three labeled **50**, **52**, and **54**, and a larger block labeled **56**. The block 56 contains two sub-components: **Tx FIFO 70** (represented by a grid of horizontal lines) and **Rx FIFO 72** (represented by a shaded grid). At the very bottom, there are four pairs of vertical lines representing connectors, and a single vertical line with an upward-pointing arrow.

F. G. 42

DMA Transfers Data from Rx FIFO to Shared System Memory

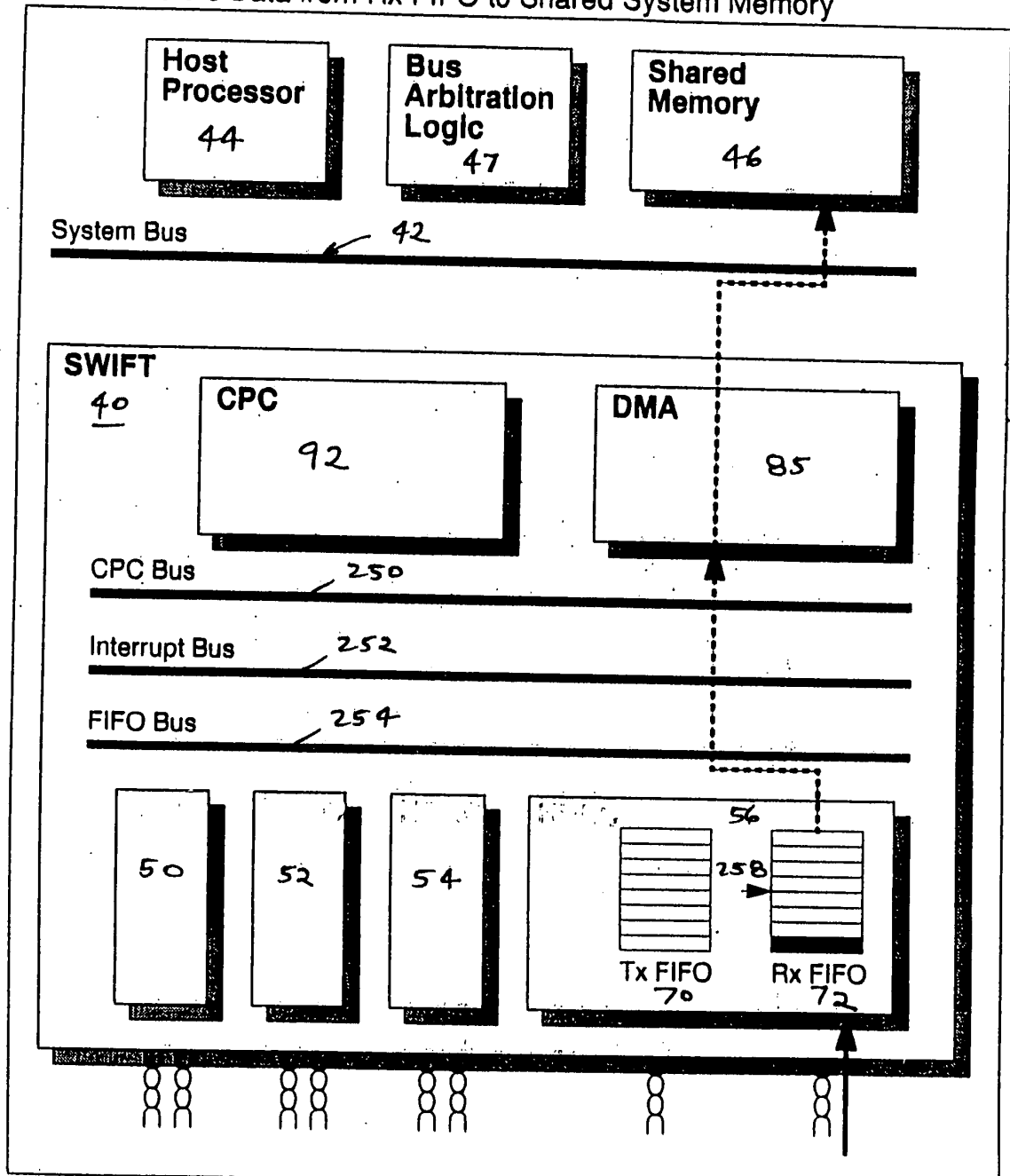


FIG. 43

Estimated Traffic Composition of the Host Bus

DATA: $X/32$
 DESCRIPTORS: $2 \cdot X/128 + 2$
 TOTAL: $X/32 + 2 \cdot X/128 + 2$

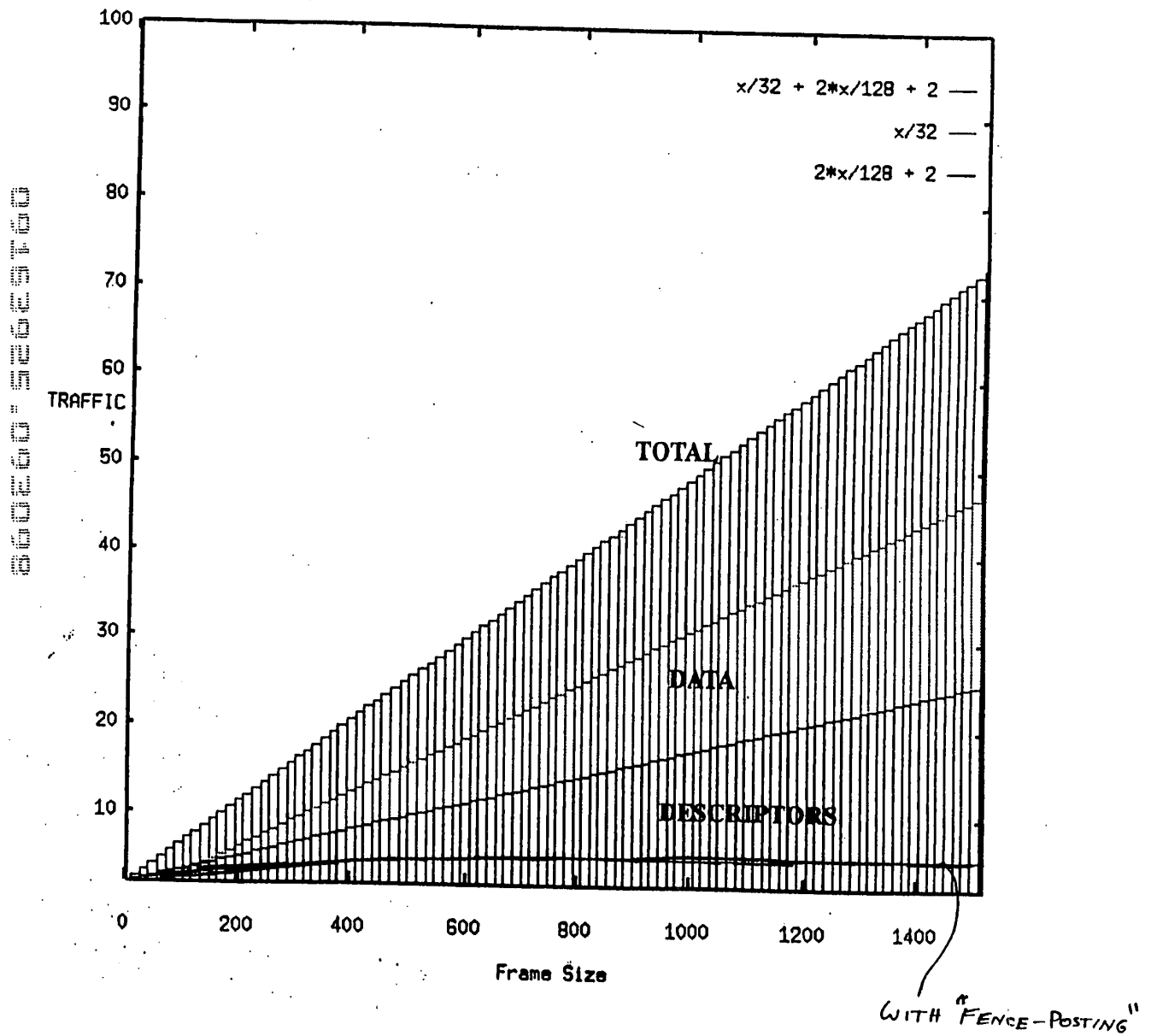


FIG. 44

Primitive Signalling

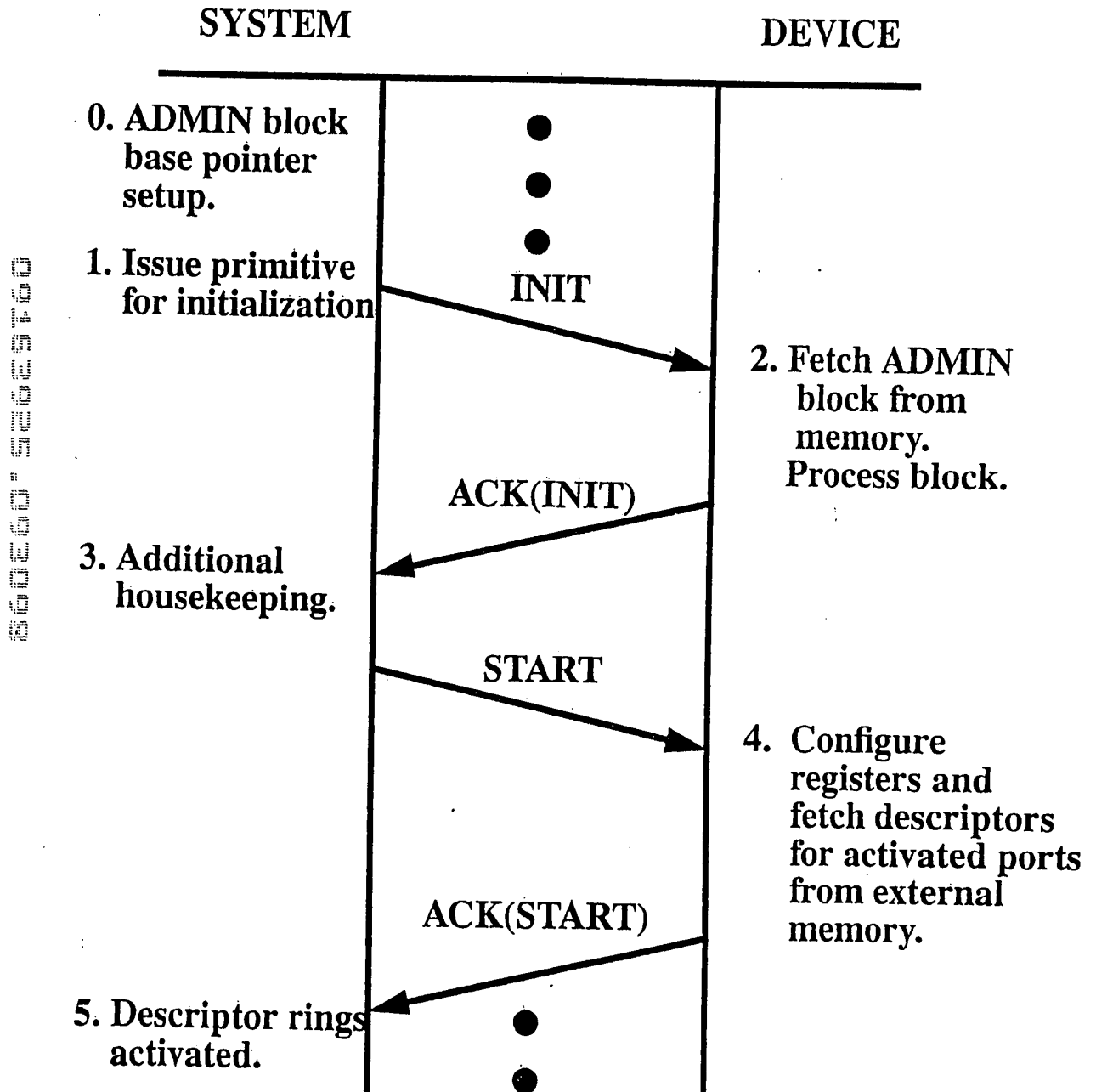
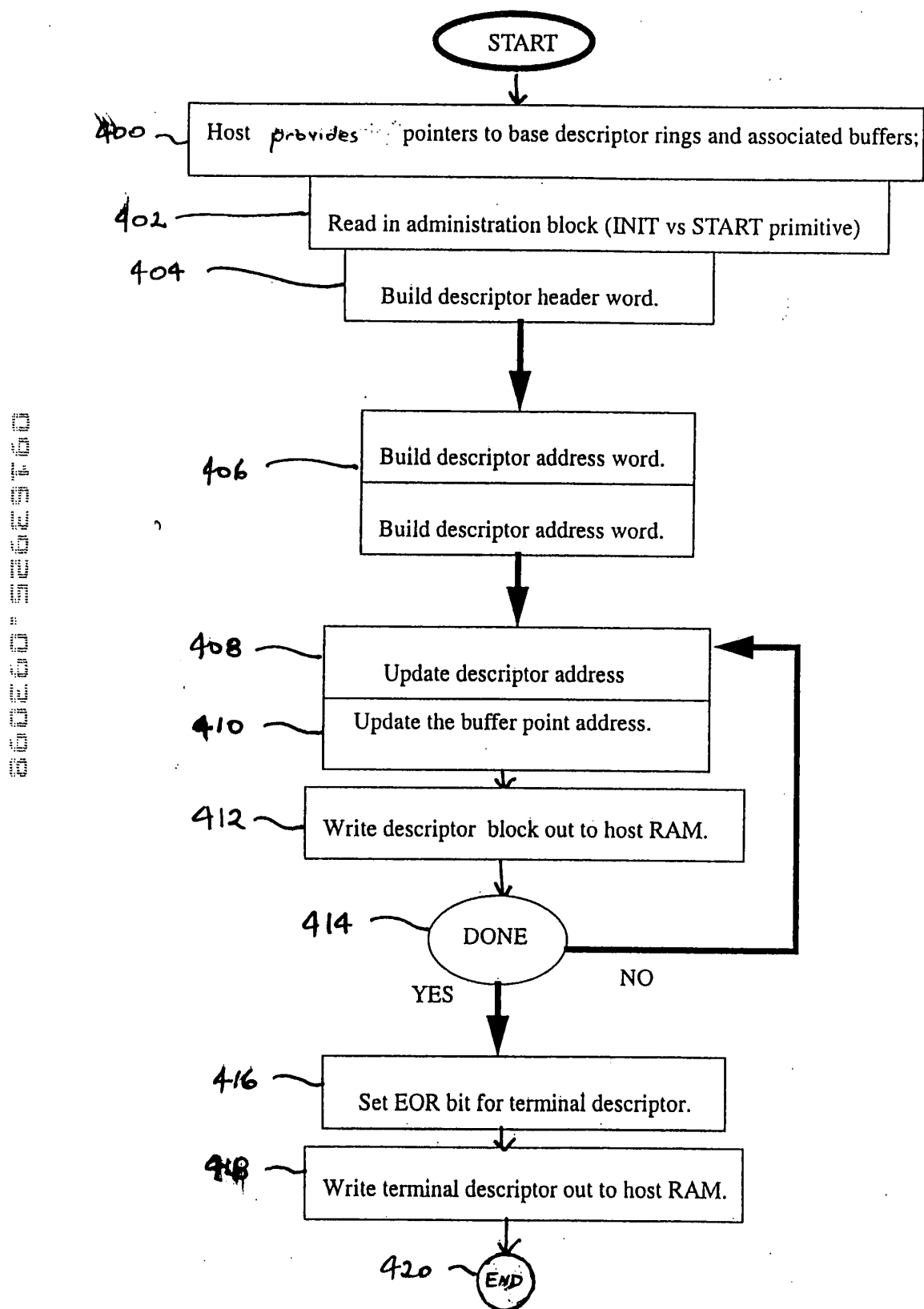


FIG. 45



60200-500000

Receive Message Descriptor 0

RMD0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	OWN	EOR	ENP	BSIZE[12:2]												RERR	ROFLO	MSIZE[12:0]														

Bit #	Field	Name	Description
31	OWN	Descriptor Ownership	(1=Device; 0=Host) Establishes ownership of the Receive Message Descriptor and its associated data buffer. The OWN bit is used as a handshake between and the host. No part of the Receive Message Descriptor or the contents of its associated buffer should be altered once ownership has been relinquished.
30	EOR	End of Ring	(1=end-of-ring; 0=not end-of-ring) Denotes the last Receive Message Descriptor in the descriptor ring. Causes Device to return to the top of the ring after using this descriptor. In other words, the next descriptor used by Device will be the first entry in the ring.
29	ENP	End of frame	(1=end-of-frame; 0=chain) Indicates the associated receive data buffer contains the end of a received frame. ENP of zero implies buffer 'chaining' where the received frame spans two or more, adjacent descriptors.
28:18	BSIZE	Buffer Size	(10-bit unsigned Integer) Indicates the number of bytes available in the associated receive data buffer (up to 8K bytes). Note that buffers are allocated in 4-byte (1-word) increments since the BSIZE field is defined as bits 12 to 2. The BSIZE field is positioned in the upper half-word to facilitate this definition. A BSIZE of zero defaults to a buffer size of one word. The actual number of bytes available in a buffer are determined by the BSIZE field and the starting address of the buffer (RBADR). Receive data buffers are permitted to start on any byte address but are always assumed by Device to end on a word-aligned boundary. In other words, the last address of every receive buffer is a complete, 4-byte word.
17	RERR	Rx Error Summary	(1=error; 0=normal) Logical OR summary of the error status bits reported in the receive status word written by Device into the first full word following the end of the frame in the buffer. RERR summarizes: CNTOVL, FCS, RABRT, ROFLO. Allows a single-bit test for receive frame-related errors.
16	ROFLO	Rx FIFO Overflow Error	(1=error; 0=normal) Indicates a dropped packet due to insufficient space available in the receive FIFO. When overflow occurs the HDLC unit continues to monitor the incoming packet for statistical purposes, and drops the entire packet (or at least the portion not yet read from the FIFO). The resulting status word is written into the FIFO along with the End-Of-Packet tag. Overflow is caused by inadequate servicing (reading) of the FIFO. If this bit is set MSIZE may not indicate the actual amount of data in the buffer.
15:0	MSIZE	Message Size	(15-bit unsigned Integer) Indicates the number of octets occupied by part or all of a received frame in the associated buffer. MSIZE does not include the four octets of the receive status word written by Device into the first full word following the end of the frame in the buffer. The MSIZE field is expected to be all zeros when the host gives ownership of the descriptor to Device. Since no attempt is made by Device to check this, any non-zero value given will result in an erroneous MSIZE returned.

FIG. 47

Receive Message Descriptor 1

RMD1	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	RBADR[31:0]																															

Bit #	Field	Name	Description															
31:0	RBADR	Receive Buffer Starting Address	<p>(32-bit unsigned integer) Acts as a pointer to the first address location of the associated receive data buffer. Receive data buffers are used by Device to store incoming frames. No more than one frame is stored in a given buffer. A single frame may span multiple buffers when its size exceeds the buffer size.</p> <p>RBADR is a byte address in a 32-bit data word system implying that receive buffers are not required to begin on word-aligned boundaries. The rule imposed by Device is that receive buffers may start with any byte alignment, but always end on word-aligned boundaries. The following table outlines the byte alignment indicated by the least two significant RBADR bits.</p> <table><tr><th>RBADR(1:0)</th><th>Valid Bytes</th><th>Alignment</th></tr><tr><td>00</td><td>4</td><td>Aligned (full word)</td></tr><tr><td>01</td><td>3</td><td>Non-aligned</td></tr><tr><td>10</td><td>2</td><td>Non-aligned</td></tr><tr><td>11</td><td>1</td><td>Non-aligned</td></tr></table>	RBADR(1:0)	Valid Bytes	Alignment	00	4	Aligned (full word)	01	3	Non-aligned	10	2	Non-aligned	11	1	Non-aligned
RBADR(1:0)	Valid Bytes	Alignment																
00	4	Aligned (full word)																
01	3	Non-aligned																
10	2	Non-aligned																
11	1	Non-aligned																

00000000000000000000000000000000

FIG. 48

Transmit Message Descriptor 0

TMD0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	OWN	EOR	ENP	NOCRC	TOFLO	Reserved										UFLO	MSIZE[12:0]															

Bit #	Field	Name	Description
31	OWN	Descriptor Ownership	(1=Device; 0=Host) Set by the host, cleared by Device. Establishes ownership of the Transmit Message Descriptor and its associated data buffer. The OWN bit is used as a handshake between Device and the host. No part of the Transmit Message Descriptor or the contents of its associated buffer should be altered once ownership has been relinquished.
30	EOR	End of Ring	(1=end-of-ring; 0=not end-of-ring) Configured by the host to mark the descriptor as the last entry in the ring. Denotes the last Transmit Message Descriptor in the descriptor ring. Causes Device to return to the top of the ring after using this descriptor. In other words, the next descriptor used by Device will be the first entry in the ring.
29	ENP	End of frame	(1=end-of-frame; 0=not end-of-frame) Set by the host to indicate that the associated transmit data buffer contains the end of a transmit frame. ENP of zero implies buffer 'chaining' where the frame to be transmitted spans two or more, adjacent descriptors.
28 ^a	NOCRC	No CRC Appended	(1=not appended; 0=appended) Configured by the host to control Tx CRC generation on a per-frame basis. Prevents Frame Check Sequence (CRC) from being generated and appended automatically by the Device unit. NOCRC is only used by Device when the End of frame (ENP) bit is set.
27	TOFLO	TX FIFO Overflow error	(1=error; 0=normal) Set by HDLC when Fifo TX is in overflow. Probably due to watermark < burst size. This means an attempt has been made to write more than the available space in the FIFO TX. The only way to exit from this condition is to set TXFLUSH or Reset.
26:17	Reserved	—	Must be zero.
16	UFLO	Tx FIFO Underflow Error	(1=error; 0=normal) Set by Device when the transmit FIFO is emptied during a transmission before encountering the End-Of-frame. Underflow is caused by inadequate servicing (writing) of the FIFO.
15:0	MSIZE	Message Size	(13-bit unsigned Integer) Set by the host to indicate the number of octets of a transmit frame contained in the associated transmit data buffer.

00163000 50005160

F. G. 49

Transmit Message Descriptor 1

TMD1	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	TBADR[31:0]																															

Bit #	Field	Name	Description															
31:0	TBADR	Transmit Buffer Starting Address	<p>(32-bit unsigned integer) Acts as a pointer to the first address location of the associated transmit data buffer. Transmit data buffers are used by Device as the source for outgoing frames. No more than one frame should be stored in a given buffer. A single frame may span multiple buffers when its size exceeds the buffer size.</p> <p>TBADR is a byte address in a 32-bit data word system implying that transmit buffers are not required to begin on word-aligned boundaries. The following table outlines the byte alignment indicated by the least two significant TBADR bits.</p> <table><tr><th><u>TBADR[1:0]</u></th><th><u>Valid Bytes</u></th><th><u>Alignment</u></th></tr><tr><td>00</td><td>4</td><td>Aligned (full word)</td></tr><tr><td>01</td><td>3</td><td>Non-aligned</td></tr><tr><td>10</td><td>2</td><td>Non-aligned</td></tr><tr><td>11</td><td>1</td><td>Non-aligned</td></tr></table>	<u>TBADR[1:0]</u>	<u>Valid Bytes</u>	<u>Alignment</u>	00	4	Aligned (full word)	01	3	Non-aligned	10	2	Non-aligned	11	1	Non-aligned
<u>TBADR[1:0]</u>	<u>Valid Bytes</u>	<u>Alignment</u>																
00	4	Aligned (full word)																
01	3	Non-aligned																
10	2	Non-aligned																
11	1	Non-aligned																

FIG. 50

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